

PUSHING THE LIMITS OF CARBON NANOTUBE TRANSISTORS

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PUSHING THE LIMITS OF CARBON NANOTUBE TRANSISTORS

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Carbon nanotubes are arrangements of carbon atoms in the form of thin, hollow tubes. Their physical and electrical properties have attracted much interest in recent years – carbon nanotubes are among the strongest materials currently known and they can perform both as active and passive components in nanoscale circuits. Their electrical properties are the focus of this thesis. The work presented here shows that carbon nanotube transistors can operate in the gate quantum limit and can be used as high-frequency mixers.

In the first experiment, an aqueous electrolyte solution was used as the gate electrode of a carbon nanotube transistor. This approach accomplishes the task of efficiently increasing the electrostatic capacitance between the nanotube and the gate via a thin, high- κ dielectric (water). The total capacitance is shown to reach the quantum limit where charging is dictated by the energy level spacing in the nanotube. Additionally, the gate coupling is nearly ideal, as found from the subthreshold swing of ~ 80 mV. The coupling results in record transconductances of ~ 7 $\mu\text{S}/\text{nm}$, a result important to applications of carbon nanotubes as chemical and biological sensors.

The second experiment measures the high-frequency properties of carbon nanotube transistors by means of frequency mixing. A dc current results from the response of the device to an ac voltage. The amplitude of the current is measured as a function of the frequency of the input, revealing the existence of a cutoff between 1 and 10 GHz. The origin of the cutoff is not completely understood yet, since it is in

order-of-magnitude agreement with the cutoff obtained from the contacts while its value does not seem to vary substantially from device to device, suggesting an external limiting factor. Despite the cutoff, the mixing response was measured up to 50 GHz. This is the highest frequency at which the electrical properties of carbon nanotubes have been measured to date.

BIOGRAPHICAL SKETCH

Sami Rosenblatt was born in Recife, Brazil. He attended Colégio Israelita Moisés Chvarts all the way to high school. He finished the last year of high school at Colégio Preparatório Integrado in December 1993. Sami entered the Bachelor's degree program in Physics at Universidade Federal de Pernambuco (UFPE) and graduated with top Honors in July 1997. He continued at UFPE in the Master's in Physics program, finishing in August 1999. During his time at UFPE, he performed research in magnetic materials in the group of Prof. Sérgio Rezende, working in close collaboration with Profs. Antônio Azevedo and Flávio Aguiar. His Master's work showed evidence for a chaotic-periodic sequence in the absorption response of yttrium-iron garnets in high-power ferromagnetic resonance experiments. Following this period, Sami entered the graduate program in Physics at Cornell University in August 1999. He worked with Ken Finkelstein at the Cornell High-Energy Synchrotron Source during the summer of 2000 developing new diffraction gratings for solid-state x-ray research. In January 2001, he joined the group of Prof. Paul McEuen, in whose lab Sami worked on his Ph.D. research.

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This thesis has finally hatched after a long incubation period. While it is certainly not the first time such a metaphor has been drawn, each individual is sure to feel it anew. For me, this experience has been a taste of what it could be like to write a great piece of text. One can only hope to live to that expectation, though only time can tell. If nothing else, one surely learns what it is like to write a *long* piece of text.

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CHAPTER 1

INTRODUCTION

1.1 Carbon nanotube history

The two naturally occurring atomic configurations of carbon are graphite and diamond. Man-made carbon forms were developed throughout history as a result of demand for new materials driven by diverse applications. The first carbon fibers were developed in the 19th century by Thomas Edison as the filament for an electric light bulb (Saito 1998), which were quickly replaced by tungsten. A renewal of interest in carbon fibers occurred in the 1950's following demand from the space and aircraft industry for strong lightweight materials with superior mechanical properties. Carbon fiber research has greatly diversified since then, with improvements made to the quality of the material and fabrication methods. Among the latter, the drive for better control of the fabrication process led to the development of catalytic chemical vapor deposition (CVD). In this method, fibers grow out of a catalyst in a chamber under controlled conditions such as feedstock gas flow and temperature.

Advancements in chemistry in the last 20 years have resulted in the synthesis of new forms of carbon with nanometer-scale dimensions. First came the *fullerenes*, also called buckyballs (Kroto, Heath et al. 1985), consisting of self-terminated spheroids made of carbon, an example being C₆₀. Years later, Iijima (Iijima 1991) reported observing “helical microtubules of graphitic carbon” by transmission electron microscopy (TEM). These tubules were micrometers long and displayed nanometer-wide diameters. They would soon be known as *carbon nanotubes*.

1.2 Electrical properties¹

In order to understand the electrical properties of a carbon nanotube, we start with graphite. Graphite has a honeycomb lattice structure and is a semimetal. This is better explained by inspecting Figure 1.1, which shows the band structure of graphene – a single sheet of atomic graphite – as a function of wavevector \mathbf{k} . Along certain directions, the band gap between the valence and conduction bands goes to zero at the Fermi level. This means that graphene behaves as a metal or a semiconductor depending on the direction of \mathbf{k} .

A single-walled carbon nanotube² can be thought of as a single sheet of graphene rolled into a tube. Due to its graphitic origins, a carbon nanotube should have mechanical and electrical properties very similar to graphite. Yet because of the nanotube being only a few nanometers in diameter, quantum-mechanical electron confinement should produce other unusual electrical properties related to one-dimensional transport. As a consequence, when graphite is rolled into a carbon nanotube, the allowed \mathbf{k} 's become locked. Nanotubes are either metallic or semiconducting depending on how they were rolled.

The electrical character of a nanotube is specified by a set of two numbers that determine the *chirality* of the nanotube. These quantities are defined from the honeycomb lattice of graphene in Figure 1.2 such that the *chiral vector* is $\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 = (n, m)$ and the chiral numbers n, m are integers (the chirality convention requires $0 \leq |m| \leq n$). The length³ of the unit vectors is a and the angle they enclose is 60° . We can express the diameter of the nanotube as:

¹ This section follows Saito (Saito 1998).

² A nanotube made of several coaxial shells is known as a multi-walled nanotube. Nanotubes with several walls may have different properties when compared to their single-walled counterparts.

³ This is approximately 2.46 Å. In comparison, the nearest-neighbor distance of two carbon atoms in graphite is 1.42 Å.

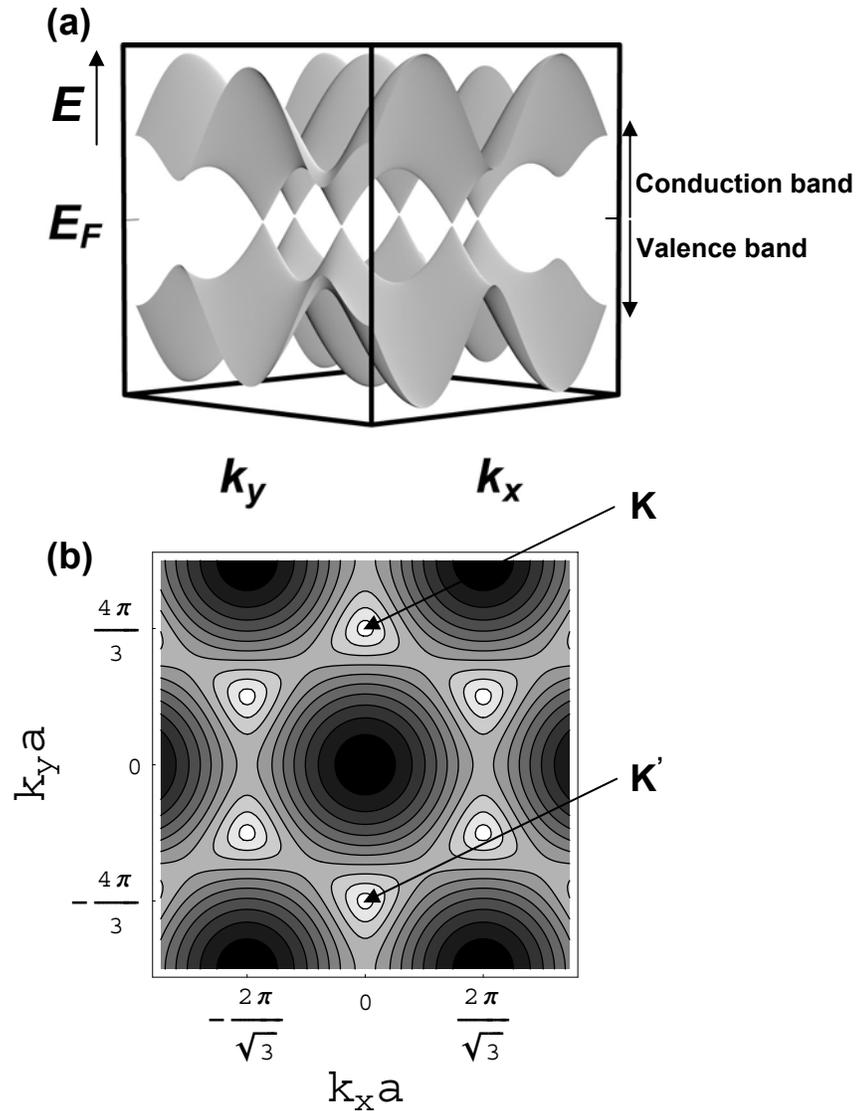


Figure 1.1. Band structure of a single graphene sheet. **(a)** 3D representation of the band structure of graphene, energy versus wavevector \mathbf{k} . The valence and conduction bands at the Fermi level meet at the so-called K points. The dispersion about these points is conical. **(b)** Contour plot corresponding to the valence band of part (a), wavevectors in units of the parameter $a = 2.46 \text{ \AA}$. Darker regions correspond to lower electron energies. The bright regions correspond to the K points. The hexagon drawn by these defines the first Brillouin zone of graphene. Two of the K points (labeled K and K') are physically inequivalent. See Saito (Saito 1998) and Minot (Minot 2004) for details.

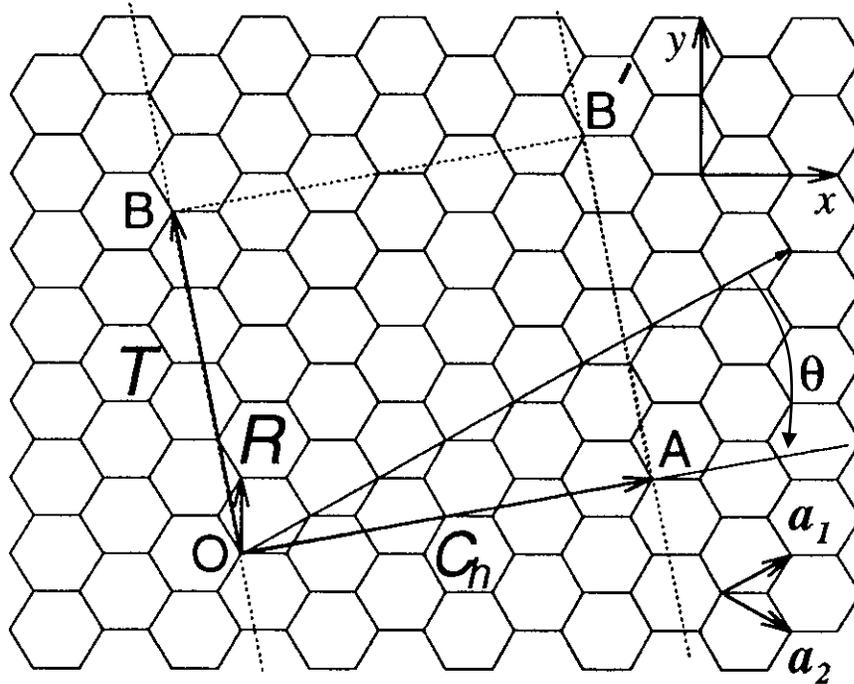


Figure 1.2. Honeycomb lattice of graphene, after Saito (Saito 1998). A nanotube can be constructed by connecting the sites O to A and B to B' . The vectors OA and OB define the chiral vector C_h . The rectangle $OABB'$ defines the unit cell for the nanotube. The chiral angle θ is measured with respect to the standard direction given in the figure (zigzag direction, see also Figure 1.3). The figure corresponds to $C_h = (4, 2)$ and tube diameter $d = 1.7a = 4.14 \text{ \AA}$. Other quantities displayed are discussed at the source reference.

$$d = \frac{|\vec{C}_h|}{\pi} = \frac{a}{\pi} \sqrt{n^2 + m^2 + nm}, \quad (1.1)$$

and we define the *chiral angle* from the figure with the expression:

$$\cos \theta = \frac{\vec{C}_h \cdot \vec{a}_1}{|\vec{C}_h| |\vec{a}_1|} = \frac{2n + m}{2\sqrt{n^2 + m^2 + nm}}. \quad (1.2)$$

Due to the hexagonal symmetry of the lattice, the chiral angle can only take on values between 0 and 30°.

When the sheet is rolled, the electron wavevector along the circumference of the nanotube is quantized. It can be shown that this condition leads to a metallic nanotube (zero band gap) only when the difference $n-m$ is a multiple of 3 (Saito 1998). Figure 1.3 illustrates the metal and semiconductor occurrence as a function of the chiral coordinates. Statistically, there should be twice as many semiconductors as there are metals (Saito 1998). Notice that the quantization condition along the circumference also predicts additional subbands. The electronic character of a nanotube (metallic or semiconducting), however, depends only on the first subband.

1.3 Carbon nanotube field-effect transistors

Experimentally, the main difference between metallic and semiconducting carbon nanotubes is in their electrical transport properties. Semiconducting nanotubes have an energy band gap in their band structure and should conduct poorly when the Fermi level lies within the gap.

The position of the Fermi level in a semiconducting nanotube can be tuned capacitively by a nearby charged conductor. This is analogous to the *gate electrode*

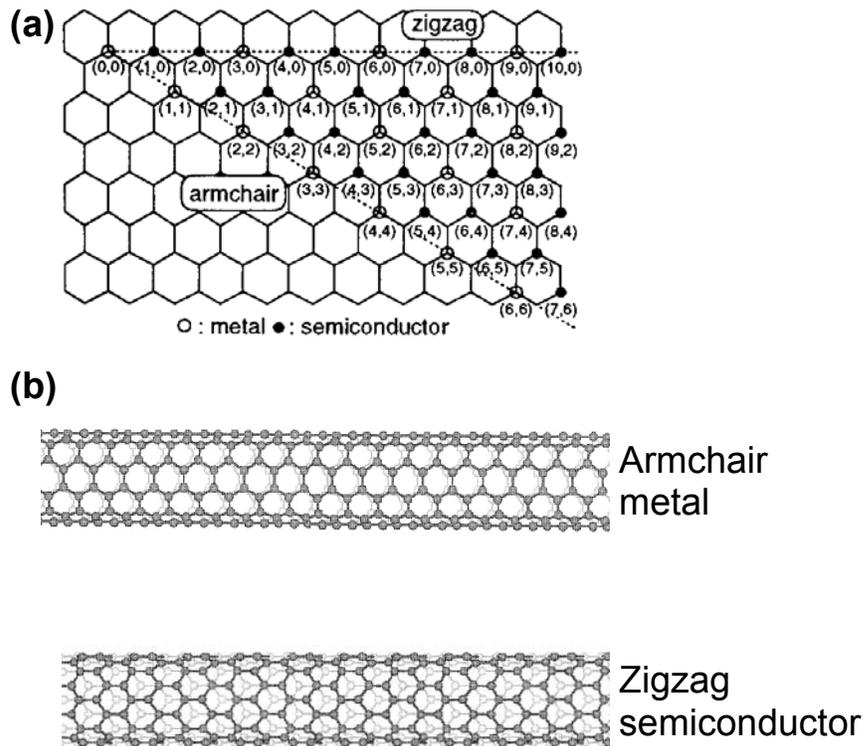


Figure 1.3. Electronic character as a function of chiral vector, after Saito (Saito 1998). (a) The possible unique ways of rolling the honeycomb lattice repeat every 30° of chiral angle. The (n, m) coordinates of the chiral vector are given at each lattice site chosen. The open circles correspond to metallic nanotubes and the dark ones correspond to semiconducting nanotubes. The zigzag direction is given its name by the way the carbon atoms alternate along that direction. The same can be said for the armchair direction – the carbon atoms appear to be drawing armchairs along that direction. All armchair nanotubes are metallic. Statistically, there are twice as many semiconducting nanotubes as metallic nanotubes. (b) Representations of an armchair nanotube (always metallic) and a zigzag semiconducting nanotube. The armchair and zigzag can be seen around the circumference of the nanotube.

of a metal-oxide-semiconductor⁴ field-effect transistor (MOSFET). Negative (positive) charge builds up in the nanotube as a result of attraction towards the positive (negative) charge in the conductor. The additional charge changes the position of the top of the valence and conduction bands relative to the Fermi level in the nanotube. Gate operation is discussed in detail in Figure 1.4.

Under typical experimental conditions, as-made nanotubes are *p-type*. They are doped with an excess of positive charge. This is attributed to nearby charges on the substrate which are left over from sample preparation (Martel, Schmidt et al. 1998). Additionally, metals such as Au make p-type contacts. For this reason, transport in semiconducting nanotubes happens primarily due to holes. Generally, it is often the case that at zero gate voltage the Fermi level is found within the valence band. Sweeping the gate voltage, however, can deplete the semiconducting nanotube and turn it off. See Figure 1.5 for an example of a semiconducting nanotube.

At larger positive gate voltage, another possibility arises that is similar to the creation of an inversion layer in a MOSFET (see Figure 1.4 (d)). Given enough positive gate voltage, the bottom of the conduction band can be pulled below the Fermi level in the nanotube. This corresponds to n-type behavior. Since the Fermi levels of the metal leads in direct contact with the nanotube tend to be within the valence band (or nearby), there is typically an intrinsic built-in barrier to n-type conduction. This results in a higher resistance to n-type transport relative to p-type transport. The band model for n-type transport is detailed in Figure 1.6 for an ambipolar device, whereas Figure 1.5 illustrates the experimental results of one such device.

⁴ In general, this is a *metal-insulator-semiconductor* junction, but we will mostly talk about oxides.

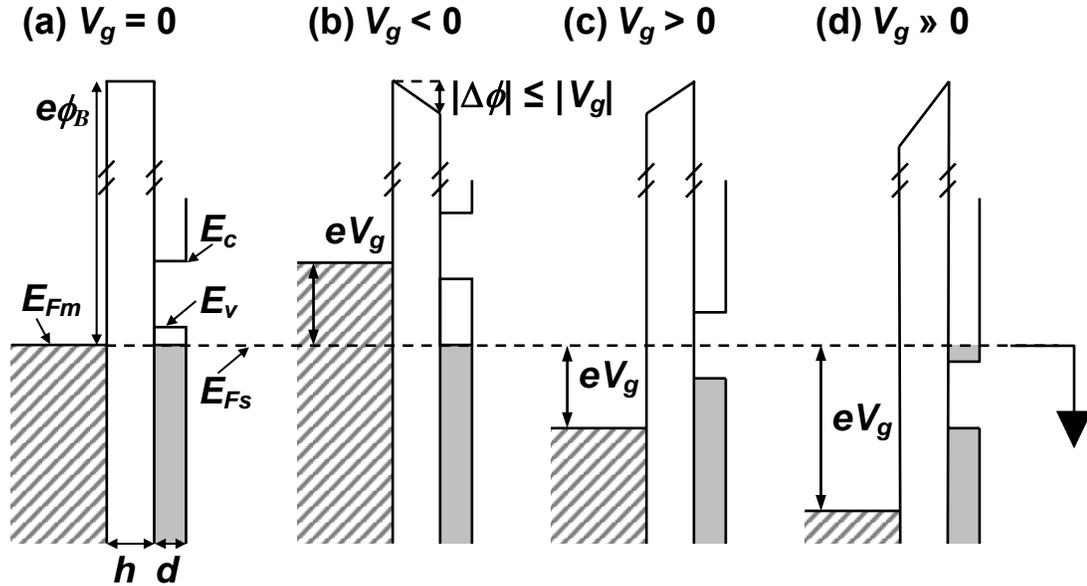


Figure 1.4. Carbon nanotube MOS capacitor band diagram. The nanotube of diameter d is represented without the metal contacts. These leads, assumed ohmic, are grounded at all times and hold the position of the Fermi level of the semiconducting nanotube, E_{Fs} , constant. A voltage V_g is applied to the gate conductor, changing the position of its Fermi level E_{Fm} . The potential barrier for electrons to cross the dielectric (of width h) from the gate conductor is ϕ_B . **(a)** Initial condition: we assume that there is no built-in potential due to the work function difference between the nanotube and the gate conductor. The Fermi levels align and no voltage drops in the dielectric. We also assume that the nanotube is heavily p-doped by its surrounding environment, so E_{Fs} is lower than the top of the valence band E_v , and there are already electronic states available for transport. **(b)** Increasing conduction by application of a negative gate voltage. The voltage drops partially in the dielectric. The nanotube becomes more positively charged, and more states are made available for conduction. **(c)** Band gap: a positive gate voltage depletes the nanotube of carriers and drives E_{Fs} into the band gap. Conduction can only happen as a result of thermally excited carriers. **(d)** N-type transport (equivalent of inversion): for sufficiently large positive gate voltage, E_{Fs} can be found above the bottom of the conduction band E_c and the nanotube behaves as an n-type FET. Tunnel or Schottky barriers at the contacts can prevent current flow. Nanotubes with appreciable p- and n-type conduction are called *ambipolar*.

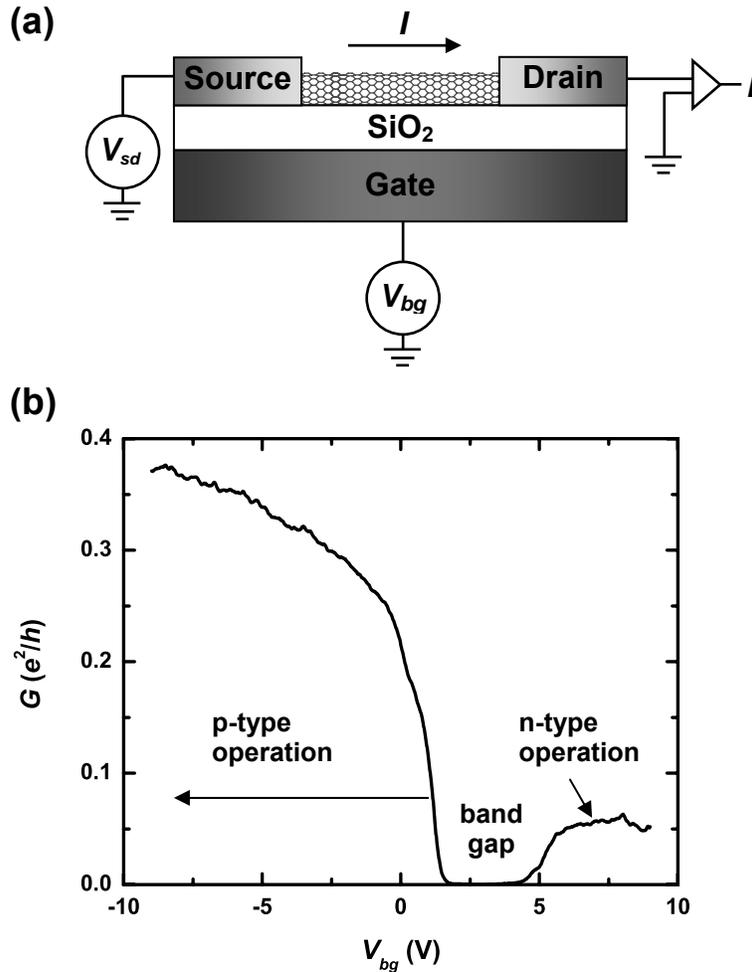


Figure 1.5. Conductance of a real ambipolar device. **(a)** Experimental setup for the measurement of the conductance of a carbon nanotube FET. The terminals are called *source* and *drain*. A voltage V_{sd} is applied to the source and the current is detected at the drain, which is connected to ground. The dielectric is SiO_2 and the conducting substrate functions as a back-gate electrode, to which a voltage V_{bg} is applied. More details about FETs will be provided in Chapter 3. Device fabrication will be discussed in Chapter 5. **(b)** Conductance in units of e^2/h ($\sim 38.8 \mu\text{S}$) versus back-gate voltage, measured at $V_{sd} = 10 \text{ mV}$. The p-type, band gap and n-type regions are indicated. Notice that the maximum n-type conductance is ~ 8 times less than the maximum p-type conductance. As explained in Figure 1.6, this is mainly due to tunnel barriers for electrons in the n-region. Since the contacts (Pd in this case) are typically p-type, there is no barrier for holes in the p-region.

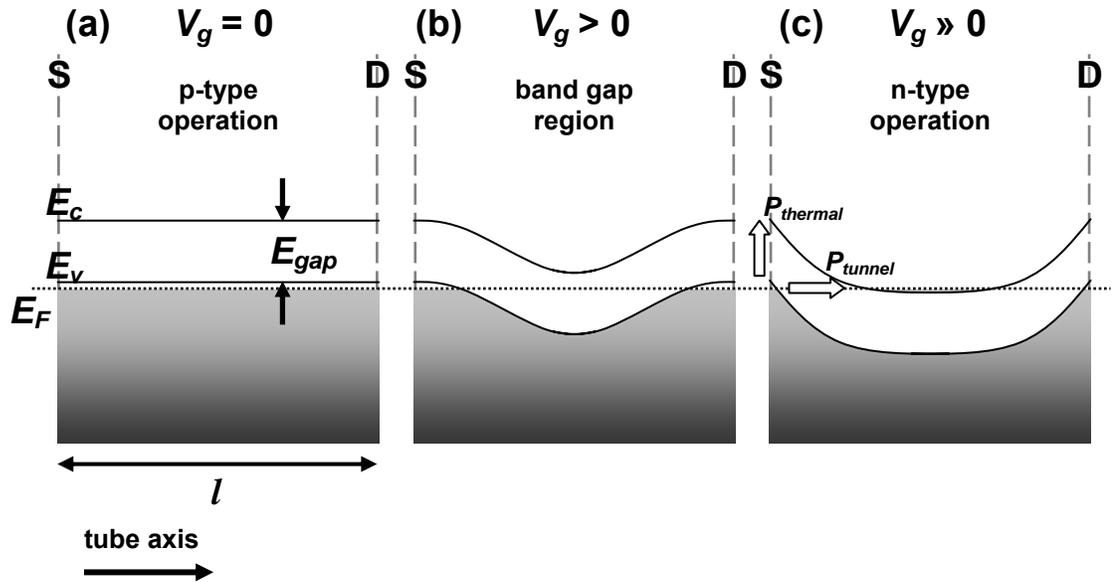


Figure 1.6. Band diagrams along the length of a carbon nanotube attached to contacts at both ends, adapted from Minot (Minot 2004). Key: E_c = conduction band edge; E_v = valence band edge; E_F = Fermi level of metal contacts; S = source contact; D = drain contact. Typical metals make ohmic p-type contacts to carbon nanotubes. Assume a similar initial condition as in Figure 1.4 for the gate capacitor and the nanotube. In this case, (a) represents zero gate voltage. There are no voltage drops either at the contact regions or in the gate dielectric. Any small bias applied between source and drain will make carriers flow across the device. Negative gate voltage pulls the bands above the Fermi level, as shown in Figure 1.4 part (b). (b) A positive gate voltage pulls the bands below the Fermi level, and the nanotube is depleted of carriers in the bulk (see Figure 1.4 (c)). Thermally activated carriers may aid transport (see discussion of the subthreshold region in Chapter 3). (c) A more positive gate voltage pulls the conduction band edge below the Fermi level (see also Figure 1.4 (d)). The main mechanisms for n-type conduction are now tunneling from valence band states to conduction band states (horizontally) and thermal activation of electrons over the band gap barrier (vertically). Both become more relevant in large-diameter nanotubes, since the band gap is inversely proportional to diameter (Saito 1998). The barrier for n-type conduction can be interpreted as a series contact resistance, explaining why experimentally observed p-type conduction is larger than n-type conduction (for p-type contacted nanotubes as in the figure). Carbon nanotubes with comparable p- and n-type conductance are called *ambipolar*. See Figure 1.5 for pertaining experimental data.

1.4 Overview of carbon nanotube field-effect transistors

To date, carbon nanotube field-effect transistors (FETs) have been produced with near-ideal properties. The two factors limiting their performance are the contact resistances and the gate capacitance. Real contact resistances have been found only a factor of two higher than the ideal value of $6.5 \text{ k}\Omega$ (Javey, Guo et al. 2003; Yaish, Park et al. 2004) when short nanotubes contacted with gold or palladium were used (see theory in Chapter 2). Although these metals were found to make p-type ohmic contacts, other groups have found carbon nanotubes to also perform as Schottky barrier transistors (Heinze, Tersoff et al. 2002; see theory in Chapter 3), a different class of devices with their own set of applications (Appenzeller, Knoch et al. 2004; Chen, Appenzeller et al. 2005; Lin, Appenzeller et al. 2005).

The gate capacitor has also been shown to operate at the ultimate quantum limit (Rosenblatt, Yaish et al. 2002; Lu, Fu et al. 2004), see e.g. Chapter 6 (see also Chapter 2 for theory). An ideal gate has important applications not only in high-performance electronics (Javey, Kim et al. 2002) but also in chemical and biological sensing (due to the high sensitivity to the surrounding electrical charges).

Furthermore, substantial progress towards air-stable n-type carbon nanotubes has been made. This is necessary in order to achieve complementary logic capabilities, such as fabricating multistage circuits that can perform operations such as NOT and NAND. One route towards this goal is to make air-stable contacts using metals with low work functions (Javey, Tu et al. 2005; Noshro, Ohno et al. 2005). A similar result can be obtained if instead the gate strongly n-dopes the nanotube (Bockrath, Hone et al. 2000; Kaminishi, Ozaki et al. 2005). This was first done by probing nanotube FETs in a chamber filled with potassium gas. In this case, the K ions strongly change the electrochemical potential of the nanotube, even near the contacts, lowering substantially the barrier for n-type conduction.

The advancements in carbon nanotube low-frequency characterization of the last few years have made it possible to turn the focus of research to high-frequency characterization. Technologically speaking, a carbon nanotube operating in the one-dimensional ballistic limit (no scattering along its length, see Chapter 2) should be able to pass high-frequency signals in the terahertz range (Burke 2002). Scientifically speaking, this operating regime has direct implications towards the experimental understanding of Luttinger liquids (Tans, Devoret et al. 1998; Bockrath, Cobden et al. 1999).

We have chosen to tackle high-frequency characterization of carbon nanotubes through their nonlinear properties using a technique called frequency mixing. Although measurements in the terahertz range are experimentally challenging, it is possible to access frequencies up to 50 GHz with standard high-frequency equipment. Furthermore, the diffusive regime of operation (dominated by scattering off the nanotube lattice) is also more accessible than the ballistic regime. As preparation for the challenges of operating nanotubes at high frequencies in ideal conditions, the experiment reported in Chapter 7 is concerned with operation of carbon nanotube FETs in the diffusive regime.

1.5 Summary and outline

Carbon nanotubes come in two flavors, metallic and semiconducting. The latter are of immediate interest towards applications in field-effect transistors and sensing. Such carbon nanotube FETs have already been made with near-ideal properties. Chapter 2 addresses the fundamental properties of carbon nanotubes. Chapter 3 presents a model for transport in a carbon nanotube FET. Chapter 4 discusses a model for the high-frequency mixer operation of these FETs. Chapter 5 presents the fabrication and standard characterization of our carbon nanotube FETs. In

Chapter 6 we deal with high-performance electrolyte-gating of carbon nanotubes as an experimental proof of the ultimate limits for dc gate operation. Chapter 7 presents and discusses the experimental results of using a carbon nanotube FET as a high-frequency mixer up to 50 GHz, the highest frequency used to date to probe a single or a few carbon nanotubes. Finally, a summary of the work and future directions is given in Chapter 8.

CHAPTER 2

ELECTRICAL PROPERTIES OF CARBON NANOTUBES

2.1 Introduction

Prior to discussing device physics and applications of carbon nanotubes, we must understand their fundamental electrical properties. This chapter marks the beginning of a three-part theoretical discussion of carbon nanotube devices. In the current chapter, we will review the basic electrical properties of carbon nanotubes. These are characterized by the resistance, capacitance and inductance of the device (see Figure 2.1). Chapter 3 will deal with carbon nanotube field-effect transistors (FETs), while Chapter 4 describes one particular kind of high-frequency application, mixing.

2.2 Nanotube density of states¹

When graphene (single-sheet graphite) is rolled into a carbon nanotube, the electron wavelength becomes quantized in the circumferential direction, giving rise to subbands of allowed electron energy states. The general² dispersion relation of the first subband is that of relativistic fermions, given by:

$$\begin{aligned} E(k) &= \pm \sqrt{(m^* v_0^2)^2 + (\hbar k v_0)^2} = m^* v_0^2 \sqrt{1 + (\hbar k / m^* v_0)^2} \\ \Rightarrow \hbar k &= \pm \frac{1}{v_0} \sqrt{E^2 - (m^* v_0^2)^2} \end{aligned} \quad , \quad (2.1)$$

¹ This section follows Datta (Datta 1997) and Kittel and McEuen (Kittel and McEuen 2005).

² Since the effective mass is given by the inverse curvature of the band, it is zero for a metallic carbon nanotube. In this case, we obtain directly that the energy is equal to the kinetic energy of the electrons in the band. The dispersion is then linear in k with slope given by the Fermi velocity in graphene.

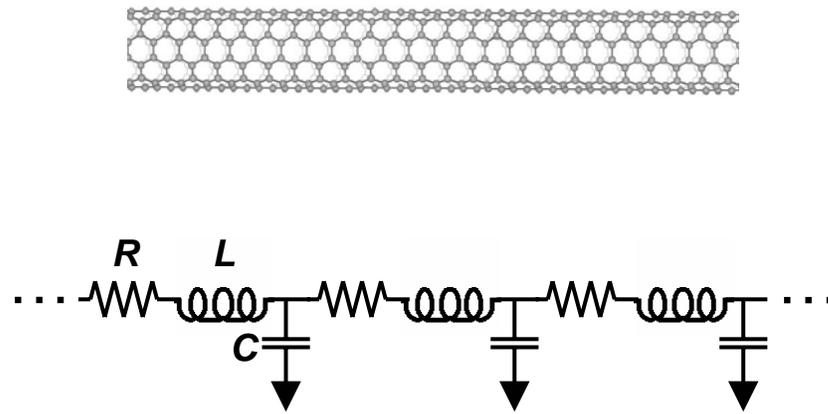


Figure 2.1. Carbon nanotube fundamental electrical parameters. We can represent the nanotube as a distributed network with a resistance R , inductance L and capacitance C (to ground) per unit length.

where $v_0 = 8 \times 10^5$ m/s, the Fermi velocity in graphene, plays the role of the speed of light and represents the velocity at high energies, k is the electron wavevector, and \hbar is Planck's constant. The effective mass (for semiconducting nanotubes) is related to the diameter d of the nanotube by³ (Saito 1998):

$$m^* = \pm \frac{2\hbar}{3dv_0}. \quad (2.2)$$

The carrier velocity is then given by:

$$\begin{aligned} v(k) &= \frac{1}{\hbar} \frac{\partial E}{\partial k} = \frac{\hbar k}{m^* \sqrt{1 + (\hbar k / m^* v_0)^2}} \\ \Rightarrow v(E) &= v_0 \sqrt{1 - \left(\frac{m^* v_0^2}{E} \right)^2}. \end{aligned} \quad (2.3)$$

Notice that the velocity becomes a constant at large energy, with $v \rightarrow v_0$.

In 1D reciprocal space, the ratio of the total region with wavevector less than the Fermi wavevector k to the level spacing⁴ gives the total number of carriers in the subband:

$$N(k) = 2 \cdot 2 \cdot \frac{2k}{2\pi/L} = \frac{4kL}{\pi}, \quad (2.4)$$

where L is the length of the nanotube, one factor of two accounts for both spins, the additional factor of 2 comes from the two sublattices of graphene⁵, and the numerator

³ The diameter determines the band gap energy, which in turn determines the parabolic behavior of the dispersion relation at low energies.

⁴ It is $2\pi/L$ in reciprocal space.

⁵ One corresponding to a bonding configuration and another to an antibonding configuration. See details in Minot (Minot 2004).

is $2k$ because this is the allowed wavevector range in one dimension (from $-k$ to $+k$). Finally, we can write the DOS per unit energy and unit length of the first subband in a nanotube using Equations 2.3 and 2.4. We obtain:

$$g(E) = \frac{1}{L} \frac{\partial N}{\partial E} = \frac{1}{L} \frac{\partial N}{\partial k} \frac{\partial k}{\partial E} = \frac{4}{\pi} \frac{1}{\hbar v} = \frac{8}{h v}. \quad (2.5)$$

At the bottom of the band $v = 0$, from which we obtain a van Hove singularity – the DOS diverges (see Figure 2.2). At high energies, the DOS is a constant due to the maximum limiting velocity. The fact that the DOS $\sim v^{-1}$ is a general property of one-dimensional systems and is applicable to quasi-1D wires as well⁶. The DOS will be a critical parameter for determining the conducting properties of the nanotube.

2.3 Conductance

We can now calculate the current flow in a perfect nanotube caused by application of a positive bias V across the conducting channel. This is given by the net density per unit length δn_e of electrons moving towards the contact with the higher voltage (or lower electron potential energy). We obtain:

$$\begin{aligned} I &= \delta n_e e v = \left(\frac{1}{2} g(E) e V \right) e v = \frac{4}{h v} v e^2 V = \frac{4e^2}{h} V, \\ \Rightarrow G_Q &= I/V = 4e^2/h \end{aligned} \quad (2.6)$$

⁶ In addition to spin, the total DOS in 1D must account for all subbands (S) and additional modes (M) up to the Fermi energy (or momentum),

$$g(E) = \sum_{S,M} g_{S,M}(E) = \sum_{S,M} \frac{4}{h v_{S,M}(E)}.$$

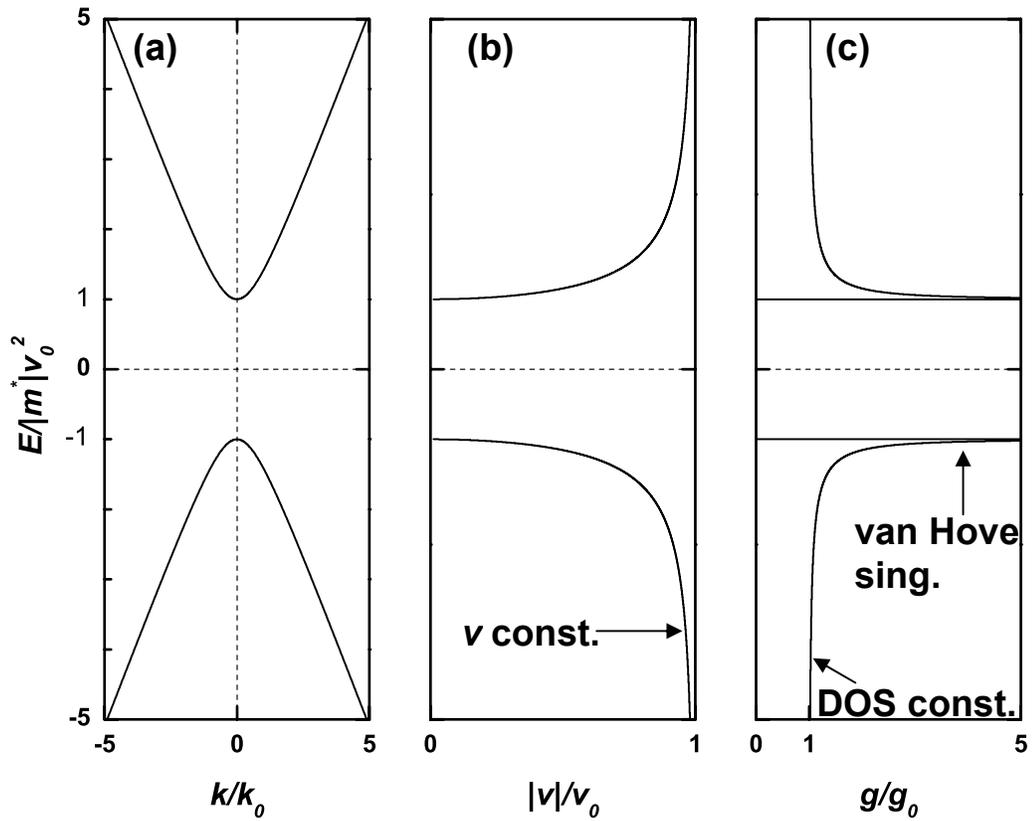


Figure 2.2. Energy versus wavevector, velocity and density of states of a semiconducting carbon nanotube. Band structure **(a)**, carrier velocity **(b)** and density of states **(c)** of the first subband of a semiconducting carbon nanotube. The energy follows a linear relation with the momentum away from the band edges, with $E \rightarrow \hbar k v_0$ (also, $k_0 = |m^*|v_0/\hbar$). Also, at high (hole or electron) energies, the velocity quickly goes to the constant value $v_0 = 8 \times 10^5$ m/s (same as Fermi velocity in graphene). Finally, the density of states (DOS) has a van Hove singularity at the band edges and quickly becomes a constant after that, with $g_0 = 8/\hbar v_0$.

where we used that the DOS of the electrons moving in one direction is $\frac{1}{2}$ of the total DOS⁷ at the Fermi level. The quantity $G_Q = 4e^2/h$ is known as the *quantum conductance* of the nanotube. Its value depends only on fundamental constants due to the exact cancellation of the carrier velocity v in 1D, and is $G_Q \approx 155 \mu\text{S}$. We often use the *quantum resistance* of the nanotube, that by definition is $R_Q = G_Q^{-1} = 6.45 \text{ k}\Omega$.

This derivation implies a transmission probability of unity through the carbon nanotube, something known as *ballistic conduction*. The voltage drop associated with the quantum resistance arises from the contacts. There is an inherent resistance to electronic flow from a 3D metal lead (high conductance) to a 1D conductor (finite conductance). We can draw an analogy with a pipeline: there is a pressure drop associated with the gas flow from a wide pipe to a narrow pipe, and the stream velocity subsequently increases (in order to maintain constant particle flow), similar to ballistic transport.

If the probability of transmission at the Fermi level $T(E)$ through the nanotube is not unity, the conductance is reduced according to the *Landauer formula*⁸:

$$G(E) = \frac{4e^2}{h} T(E). \quad (2.7)$$

We can use this result to rewrite the resistance of a nanotube as:

$$R = G^{-1} = \frac{h}{4e^2} \frac{1}{T} = \frac{h}{4e^2} + \frac{h}{4e^2} \frac{\Gamma}{T}, \quad (2.8)$$

⁷ Take either $k > 0$ or $k < 0$, for instance, in Equations 2.4 and 2.5.

⁸ If there are multiple channels or subbands, their conductances add in parallel, such that the equivalent transmission probability is given by (i and j are the corresponding quantum numbers):

$$T(E) = \sum_{i,j} T_{ij}(E).$$

where Γ is the reflection probability and $T+\Gamma = 1$. This shows the two contributions to the resistance. The first term is the quantum resistance, while the second term corresponds to resistance from scattering in the nanotube.

Both of these contributions are important when studying transport in carbon nanotubes. In particular, for incoherent, diffusive propagation⁹, the scattering term reduces to Ohm's law in one dimension, a classical result. We can associate a mean free path l_0 with it to quantify the probability of scattering. Then, Equation 2.8 can be written as a series combination of the quantum and classical resistances:

$$\begin{aligned} R &= R_Q + R_{\text{Classical}} \\ &= \frac{h}{4e^2} \left(1 + \frac{L}{l_0} \right). \end{aligned} \quad (2.9)$$

When $l_0 \ll L$, the classical resistance dominates. In the ballistic limit, on the other hand, $l_0 \gg L$ and this Equation reduces to the quantum result of Equation 2.6. The ballistic conduction limit has been observed at low temperatures¹⁰ in well-contacted (transparent contacts with low contact resistances) and short nanotubes (Kong, Yenilmez et al. 2001). Room-temperature measurements have come to within a factor of 2 of this limit (Javey, Guo et al. 2003).

2.4 Capacitance

We will now see that the DOS of the carbon nanotube limits the amount of charge that can be statically added to the device: the capacitance of the nanotube has a quantum component as well as a classical one. The electrostatic classical part C_E is a result of the electric field between conductors, and thus depends on the geometry and

⁹ Electrons lose phase information in between collisions. See Datta (Datta 1997) and Kittel (Kittel and McEuen 2005).

¹⁰ In order to minimize scattering by acoustic phonons.

the dielectric surroundings. On the other hand, the chemical/quantum part C_Q is a result of the constraints introduced by the discrete electronic states and should be directly related to the DOS and independent of electrostatics.

Let us start by defining this DOS contribution. The amount of energy required to add one electron to the next available k -state of a carbon nanotube is calculated using Equation 2.5 as follows:

$$\frac{\delta E}{\delta N} = \frac{g^{-1}(E)}{L} = \frac{hv}{8L}, \quad (2.10)$$

We can then calculate a capacitance per unit length (prime denotes *per unit length*) for adding an amount of charge $\delta q = \delta Ne$ in the usual way¹¹:

$$C_Q' = \frac{1}{L} \frac{\delta q}{\delta(E/e)} = e^2 g(E) = \frac{8e^2}{hv}. \quad (2.11)$$

This is the *quantum capacitance*¹². We see that it is directly proportional to the DOS. In the limit $v \rightarrow v_0 = 8 \times 10^5$ m/s we obtain $C_Q' \rightarrow C_{Q0}' \approx 3.86 \times 10^{-16}$ F/ μ m. Notice that due to the van Hove singularity in the DOS, $C_Q' \rightarrow \infty$ at the band edge.

If the nanotube is deposited on a conducting substrate with a dielectric in between, there exists an electrostatic contribution to the capacitance. We will just quote the value of the capacitance between a wire and a ground plane (Ramo, Whinnery et al. 1984):

¹¹ Using that $C = dq/dV$, by definition. Dividing E by e results in the electric potential (neglecting the sign).

¹² In this derivation, four modes were taken into account in Equation 2.10, two from spin and two from the sublattices of graphene. The quantum capacitance per mode is $C_Q'/M = 2e^2/(hv)$.

$$C'_E = \frac{2\pi\kappa\epsilon_0}{\cosh^{-1}(2h/d)} \approx \frac{2\pi\kappa\epsilon_0}{\ln(4h/d)}, \quad (2.12)$$

where κ is the relative dielectric constant, $\epsilon_0 = 8.85 \times 10^{-12}$ F/m is the permittivity of vacuum, h is the distance from the center of the wire to the plane and d is the diameter of the wire. We used that $\cosh^{-1}x = \ln[x+(x^2-1)^{1/2}] \approx \ln[2x]$ for large x (distance from plane much larger than diameter of wire) in order to approximate the expression.

For practical purposes, let us assume $h = 200$ nm, $\kappa \sim 4$, $d = 2$ nm (typical parameters for silicon dioxide insulator and nanotube diameter). Then Equation 2.12 gives us $C'_E \sim 3.7 \times 10^{-17}$ F/ μm . This is within a factor of 10 of C_{Q0}' . A perhaps surprising result comes when instead $h = 10$ nm: $C'_E \sim 7.4 \times 10^{-17}$ F/ μm , just twice the capacitance of the thicker dielectric despite it being two orders of magnitude thinner. This is a consequence of the logarithm. It shows that the only effective way of increasing the capacitance is by choosing a different dielectric with higher κ .

In the special case in which the outer conductor surrounds evenly the wire, we can use the textbook result of the capacitance of a coaxial cable:

$$C'_E = \frac{2\pi\kappa\epsilon_0}{\ln(2h/d)}. \quad (2.13)$$

As will be seen in Chapter 5, a wrap-around dielectric/conductor described by this Equation can be implemented by use of a liquid or gel electrolyte. These comprise of ions (dissociated salt) dissolved in a liquid or gel matrix. Let us look at salty water, for example. Bulk water has a dielectric constant of ~ 80 at room temperature¹³, quite large compared to silicon dioxide (~ 4). When ions are dissolved into water, their equilibrium distribution establishes the *Debye screening length* λ_D . In general,

¹³ Bulk value. Actual value could be lower by a factor of 2 (Teschke, Ceotto et al. 2000).

$$\lambda_D = \sqrt{\frac{\kappa \epsilon_0 k_b T}{e^2 \sum_i c_i^b z_i^2}}, \quad (2.14)$$

where $k_b = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, T is the absolute temperature, c_i^b is the concentration of the i th ionic species in the bulk of the water, and z_i is the valence number of the i th species. The electrical potential in the water can be extracted by combining Poisson's equation with a Boltzmann distribution of the charged species in solution (Grattarola and Massobrio 1998). The main result is that the potential decays exponentially away from a conducting plane held at a potential V relative to the water (ground) with the characteristic Debye length, as $\phi(x) = V \cdot \exp(-x/\lambda_D)$. This shows that the greatest voltage drop occurs over a distance equal to one Debye length from the conductor. In the case of a nanotube, this is equivalent to having a cylindrical capacitor with the outer shell radius $h = (d/2) + \lambda_D$. For NaCl, a common salt, Equation 2.14 reduces to:

$$\lambda_D = 0.30 \text{ nm} / \sqrt{X}, \quad (2.15)$$

where X is the *molar* concentration of the salt¹⁴. For a 10 mM solution of NaCl, $\lambda_D = 3$ nm, and Equation 2.13 gives us (for $d = 2$ nm) $C_E' \sim 3.2 \times 10^{-15}$ F/ μm , roughly a factor of 10 *larger* than C_{Q0}' .

Because the quantum and electrostatic capacitances compete with each other directly for the charge filling the electronics levels, their addition rule is that of

¹⁴ Even pure water has an ionic character, since a small fraction of the molecules dissociate. The concentration of H^+ ions equals that of OH^- ions in equilibrium with 10^{-7} M (which in turn specifies the neutral pH of a solution). The Debye length using Equation 2.15 is ~ 1 μm .

capacitors in series¹⁵: $C_{total} = (C_Q^{-1} + C_E^{-1})^{-1}$. This rule predicts that the *smaller* of the two contributions will dominate. This can be better understood from Figure 2.3. When SiO₂ is used as the dielectric, C_E' dominates the total capacitance except at short distances, when it becomes comparable to C_{Q0}' . If a high dielectric constant material such as water is used, then $C_E' > C_{Q0}'$ and $C'_{total} \rightarrow C_{Q0}'$. The quantum capacitance then corresponds to the ultimate charging limit of a nanotube. In Chapter 5, we will show by means of a liquid electrolyte that this limit can be reached.

2.5 Inductance

We will now study the inductive effects of a nanotube. Conceptually, an inductance opposes a change in the current. By means of inductive effects, a current lags in phase with its response to an external field. Similarly to the conductance and the capacitance, there will be a classical and a quantum contribution to the inductance.

Classically, Faraday's law of induction states that a change in the flux of magnetic field through a conducting loop causes a voltage to build up around it. This voltage produces a current that in turn produces an opposing flux, offering resistance to the original flux change. If the magnetic flux through the loop is generated by electric current, the voltage drop around the loop is related to the current according to $V = L_M dI/dt$. We will call the proportionality factor between the voltage and the current change that originates from Faraday's law the *magnetic inductance* in order to distinguish it from the other inductive component that we will talk about. As we did with the electrostatic capacitance, we will quote the result of the magnetic inductance

¹⁵ The rigorous demonstration of the capacitance addition rule is as follows. We define the *electrochemical potential* as $\mu_E = E_F + eV$, where V is the electric potential. By definition, the capacitance is calculated as the inverse of the change in μ_E when an amount of charge δq is added:

$$C_{total}^{-1} \equiv \frac{\delta(\mu_E/e)}{\delta q} = \frac{\delta(E_F/e)}{\delta q} + \frac{\delta V}{\delta q} \equiv C_Q^{-1} + C_E^{-1}.$$

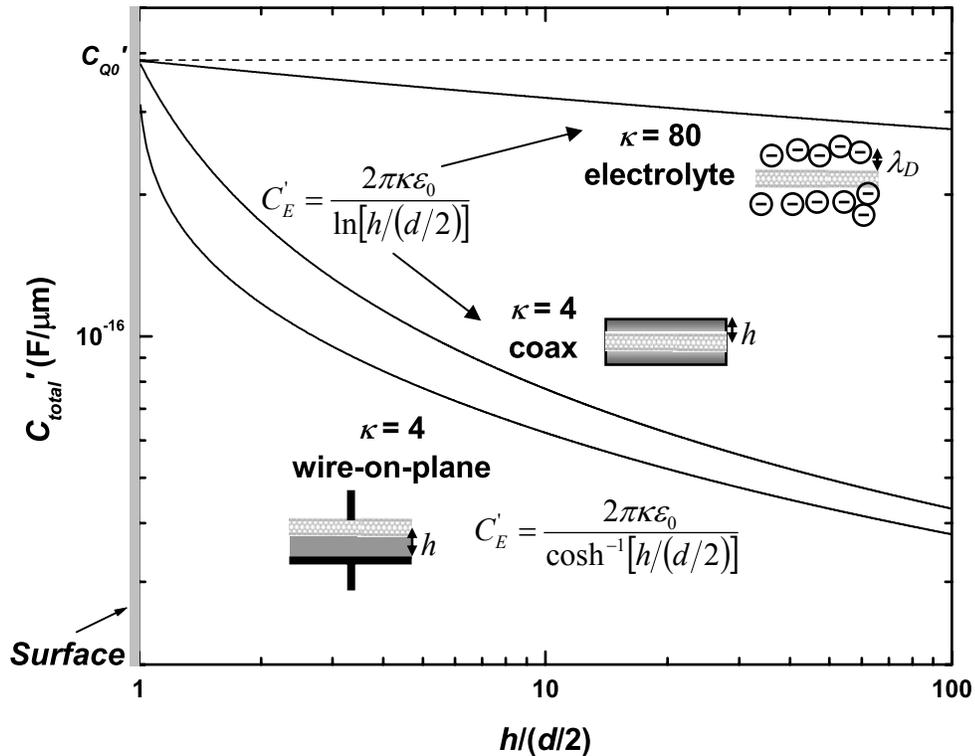


Figure 2.3. Total capacitance per unit length of a carbon nanotube versus distance. The distance from the axis of the nanotube's cylinder to the surface of the other conductor is h , and the radius of the nanotube is $(d/2)$. When the insulator is silicon dioxide ($\kappa \sim 4$), the electrostatic capacitance dominates the total capacitance, except for a gate very near the surface of the nanotube. On the other hand, the electrolyte configuration should have the quantum capacitance of the nanotube dominate the total capacitance, even at low concentrations – the concentration determines the Debye screening length through Equation 2.14, which relates to the distance h through $h = (d/2) + \lambda_D$. This might be an overstatement due to the fact that the dielectric constant of the electrolyte is lower than the one in the bulk at short distances. The limiting value $C_{Q0}' = 3.86 \times 10^{-16} \text{ F}/\mu\text{m}$ is shown by a dotted line.

L_M' (per unit length) of a wire of diameter d in proximity with a ground plane a distance h away from the wire's axis (Ramo, Whinnery et al. 1984):

$$L_M' = \frac{\mu}{2\pi} \cosh^{-1}\left(\frac{2h}{d}\right) \approx \frac{\mu}{2\pi} \ln\left(\frac{4h}{d}\right). \quad (2.16)$$

The magnetic permeability of the medium is μ , which we will consider non-magnetic ($\mu = \mu_0 = 4\pi \times 10^{-7} \text{ N A}^{-2}$). For $d = 2 \text{ nm}$, $L_M' \sim 1.2 \times 10^{-3} \text{ nH}/\mu\text{m}$ when $h = 200 \text{ nm}$ and $L_M' \sim 6 \times 10^{-4} \text{ nH}/\mu\text{m}$ when $h = 10 \text{ nm}$ – it increases with distance.

At the electronic level, an additional inductance exists that can be regarded as a resistance to a change in kinetic energy of the electrons in the conductor. Such opposition would make the electrons' velocities lag in phase with regard to the external field. This quantum inductance is called *kinetic inductance* due to its origins. First, we consider the electric force acting on all the electrons in the carbon nanotube when a voltage V is applied (simply Newton's law):

$$nL \frac{eV}{L} = \frac{dP}{dt} \Rightarrow V = \frac{1}{en} \frac{dP}{dt} = \frac{h}{8em^*v} \frac{dP}{dt}, \quad (2.17)$$

where P is the total momentum of the electrons, n is the total number of electrons in the nanotube per unit length L (determined by the Fermi energy), and we used Equation 2.4 and that the Fermi wavevector is related to the Fermi velocity¹⁶ by $\hbar k = m^* v$, where m^* is the effective mass in the band.

The total momentum acquired by the electrons through application of the electric field is simply $m^* v_d$ per electron, where v_d is the drift velocity, so that:

¹⁶ For consistency, we refer to the Fermi wavevector and velocity without a subscript.

$$P = nLm^* v_d . \quad (2.18)$$

This can be related to the electric current I produced by the electric field by:

$$I = nev_d = Pe/Lm^* , \quad (2.19)$$

which we substitute into Equation 2.17 to end up with:

$$\begin{aligned} V &= L \frac{h}{8e^2 v} \frac{dI}{dt} = L'_K L \frac{dI}{dt} , \\ \Rightarrow L'_K &= \frac{h}{8e^2 v} , \end{aligned} \quad (2.20)$$

which concludes our derivation of the kinetic inductance L'_K (per unit length, hence the prime). We obtain $L'_{K0} \sim 4$ nH/ μm for the four modes of a nanotube¹⁷ in the limit $v \rightarrow v_0 = 8 \times 10^5$ m/s (corresponding to high energies or metallic nanotubes). Also notice that L'_K is proportional to v^{-1} , and therefore to the DOS. It diverges at the band edge.

The magnetic and kinetic inductances follow the addition rule of inductors in series, that is, $L_{total} = L_K + L_M$. This means that the *larger* contribution dominates.

The value that we calculated for the magnetic inductance in typical experimental conditions is several orders of magnitude lower than the kinetic

¹⁷ For one mode,

$$L'_K = \frac{h}{2e^2 v_0} ,$$

which equals to 16 nH/ μm in the ballistic regime or at high energies. Notice that since the different modes of propagation conduct in parallel, the inductances per mode also add as inductors in parallel.

inductance. The kinetic inductance is *always*¹⁸ the dominant inductance in a carbon nanotube¹⁹.

The inductive effect causes electrons to travel in the bulk as they would in a transmission line (more on this in Chapter 4). A ballistic nanotube would correspond to a lossless line, with characteristic impedance Z_0 and wave velocity v that depend on its capacitance and inductance, $Z_0 = [L/C]^{1/2}$ and $v = [L \cdot C]^{-1/2}$. The wave velocity of the plasma waves in the nanotube would generally be larger than the Fermi velocity, except in the quantum capacitance limit, when $v = v_0 = [L_{K0}C_{Q0}]^{-1/2}$. In general, v_0 is *smaller*²⁰ than the plasmon velocity by a constant factor g , which characterizes the effect of electron-electron interactions (that is, the amount by which electrostatics changes the capacitance). Tunneling experiments have put the value of g at ~ 0.3 in carbon nanotubes (Bockrath, Cobden et al. 1999; Postma, Teepen et al. 2001), but no direct evidence of measurement of the kinetic inductance has yet been made. The main obstacle is that until recently it was not possible to obtain nanotubes of suitable length which could be practically probed as transmission lines at experimentally feasible frequencies. Long nanotubes are now routinely grown (Huang, Cai et al. 2003), and some groups have proposed different techniques to probe them at high frequencies (Appenzeller and Frank 2004; Yu and Burke 2005). We have developed a technique which is very promising towards achieving this ultimate goal, as described in Chapter 7.

¹⁸ Using Equation 2.16, we only arrive at $L_M = L_K$ for $\ln(h/d) \sim 20000$, which for $d = 2$ nm implies $h \sim 10^{10000}$ nm!!! That is much larger than the observable universe (of order 10^{24} km) by any measure.

¹⁹ There is little to be gained from a wrap-around geometry such as that of an electrolyte capacitor. The medium is non-magnetic and all potential for improvement is in the logarithmic function.

²⁰ Notice that the total capacitance is generally *less* than the quantum capacitance, increasing the plasmon velocity in turn.

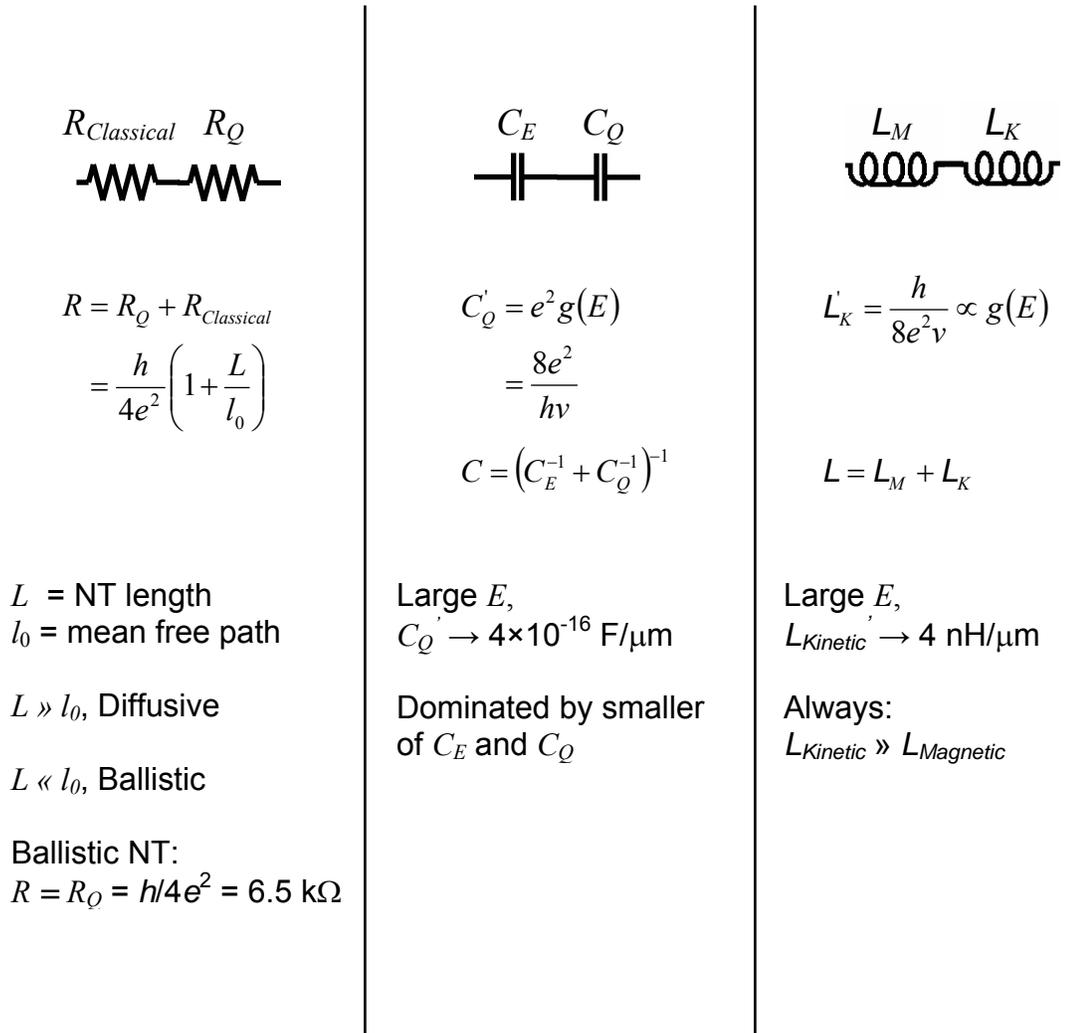


Figure 2.4. Summary of the electrical properties of a carbon nanotube.

2.6 Conclusions

As 1D systems, carbon nanotubes possess several unusual properties – quantum resistance, quantum capacitance and kinetic inductance (see Figure 2.4):

- a) The quantum resistance is a direct result of a “funnel” effect, in which a large number of electrons living in 2D or 3D metal contacts flow into a 1D system. This resistance exists even if the bulk 1D material is ballistic, and it should correspond to the ultimate limit for conduction. When incoherent scattering in the bulk dominates the resistance, though, the nanotube operates in the diffusive limit. This will be our assumption in developing the theory of the next two chapters.
- b) The quantum capacitance is a chemical limit to the ability to add charge to the nanotube. Under appropriate circumstances, such as a high- κ insulator or optimal geometry, it becomes the dominant mechanism that limits charge accumulation. We will see direct evidence of the quantum capacitance in Chapter 6.
- c) The kinetic inductance is associated with the inertia of the electrons in the nanotube. It limits the ability to change a current under a sudden increment of the applied bias. The kinetic inductance is *always* stronger than its magnetic counterpart in a carbon nanotube, and it should be relevant at high frequencies.

The resistance and the capacitance dictate the operation of carbon nanotubes as field-effect transistors (FETs), which will be the subject of next chapter. The kinetic inductance will not be addressed in our experiments, but we will comment on its consequences briefly in Chapter 4.

CHAPTER 3

THEORY OF CARBON NANOTUBE FIELD-EFFECT TRANSISTORS

3.1 Introduction

In the previous chapter, we have discussed the electrical properties that are likely to play a role in transport in nanotubes. In this chapter, we will quantify the use of semiconducting nanotubes as the active ingredient of field-effect transistors (FETs). The resistive and capacitive properties of semiconducting carbon nanotubes will be used to predict their low-frequency performance in this particular application.

3.2 Generic one-dimensional field-effect transistor

In this section, we will derive the transport characteristics of a 1D field-effect transistor (FET). The initial derivation corresponds to the general case of a diffusive one-dimensional material and is similar to the derivation of a 3D FET. Special attention to p-type FETs will be given, since this relates directly to carbon nanotube operation. In Section 3.3, a more accurate model applying the band structure properties derived in Chapter 2 will be used to describe carbon nanotube FETs in particular. Nonetheless, the methods and results obtained via the study of a generic 1D FET will constitute the basis for analysis of transistor operation.

3.2.1 Linear region

An FET can be interpreted as a variable conductor, in which the number of carriers at the semiconductor's interface is a function of the voltage V_g applied to the gate electrode. This is the geometry of a metal-oxide-semiconductor (MOS) capacitor, as introduced in Chapter 1. A voltage threshold V_{g0} separates the operation modes. For

a p-type FET, the off-state (zero conductance) is characterized by $V_g > V_{g0}$. At $V_g \leq V_{g0}$, the semiconductor starts to look like a conductor, and the total charge per unit length is given by

$$q = ne = C'_g |V_g - V_{g0}| = C'_g V_o, \quad (3.1)$$

where n is the charge density per unit length, $C'_g = C_g/L$ is the gate capacitance per unit length, and V_o will be referred to as the *gate overvoltage* (semiconductor is *grounded*). A p-type FET with $V_{g0} \leq 0$ is said to be normally off or in *enhancement* mode; otherwise, it is normally on or in *depletion* mode.

In order to include transport in this description, we must consider how the local charge density is affected by the potential landscape induced by the bias voltage applied between the terminals, called *source* and *drain*. Intuitively, a *positive* voltage V locally applied to the semiconductor side of the gate capacitor will *increase* the potential difference between the two plates of the gate capacitor (just as with a MOS capacitor), and we end up, locally, with (gate electrode is at fixed overvoltage):

$$q(x) = n(x)e = C'_g (V_o + V(x)), \quad (3.2)$$

where x is the distance measured relative to the *biased* end of the semiconductor. Assume all metal contacts have low resistance and are *ohmic*.

We can now write Ohm's law for this device (diffusive regime):

$$j = \sigma(x)\mathcal{E}(x) = (n(x)e\mu_h) \left(-\frac{\partial V(x)}{\partial x} \right), \quad (3.3)$$

where j is the current density in 1D, σ is the 1D conductivity, ε is the electric field and μ_h is the hole mobility. Notice that because the current density is a constant for the device (since there is no alternate path for the current at dc), the product between σ and E implies a constraint to the voltage profile $V(x)$. Also notice that the conductivity has dimensions of length/resistance in one dimension.

Next, we calculate the actual current flow from source to drain. The current density is numerically equivalent to the current in one dimension, so $I_{sd} \equiv j$. In order to eliminate specific knowledge of $V(x)$ in Equation 3.3, we integrate both sides of the Equation from source ($x = 0$) to drain ($x = L$), with the boundary conditions $V(0) = V_{sd}$ and $V(L) = 0$ ¹ (which gives the desired convention that positive current flows towards the more negative terminal):

$$\begin{aligned} I_{sd}L &= -\mu_h C'_g \int_0^L (V_o + V(x)) \frac{\partial V(x)}{\partial x} dx \\ &= \mu_h C'_g \int_0^{V_{sd}} (V_o + V) dV \\ &= \mu_h C'_g (V_o + \frac{1}{2} V_{sd}) V_{sd} \end{aligned} \quad (3.4)$$

This result states that the correction to the carrier concentration due to the source-drain bias is given by addition of the average bias between source and drain to the overvoltage. For $|V_{sd}| \ll V_o$, the current depends linearly on the bias voltage V_{sd} . This is

¹ The textbook convention for biasing a p-type FET is that the source is *grounded* while the drain is kept at a *negative* bias V_{ds} . The reason for doing this is that the FET saturation mode, of interest for applications, can only be reached through pinch-off, when $V_{ds} = -V_o$. The biasing convention ensures that the current still flows from source to drain. For $V_{ds} < 0$, the current flowing from *source* to *drain* is given by:

$$I_{sd} = -\frac{\mu_h C'_g}{L} (V_o + \frac{1}{2} V_{ds}) V_{ds} .$$

We see that the carrier density is now *lowered* by the average potential along the device. This is the appropriate expression for comparison with standard textbooks.

called the *linear region*. The current versus bias characteristics of the p-type 1D FET are shown in Figure 3.1 (a).

The voltage profile can now be calculated by performing integration of Equation 3.3 from 0 to x (or for V_{sd} dropping to the value $V(x)$ instead of 0) and using the result of I_{sd} of Equation 3.4. We arrive at:

$$V(x) = V_o \left(-1 + \sqrt{1 + 2(1 - x/L) \left(1 + \frac{1}{2} \frac{V_{sd}}{V_o} \right) \frac{V_{sd}}{V_o}} \right). \quad (3.5)$$

At small bias ($|V_{sd}| \ll V_o$), Equation 3.5 becomes simply a linear profile:

$$V(x) = (1 - x/L)V_{sd}. \quad (3.6)$$

The voltage profile in the p-type 1D FET is shown in Figure 3.1 (b).

We can calculate the conductance of the device from its definition, $G \equiv I_{sd}/V_{sd}$, and we obtain^{2,3}:

$$G = \frac{\mu_h C'_g}{L} \left(V_o + \frac{1}{2} V_{sd} \right). \quad (3.7)$$

² In this version, the contacts are assumed to have low resistance, resulting in little additional voltage drop. The voltages applied to the contact regions are, therefore, the same voltages experienced by the device.

³ The standard textbook derivation of these equations (3D case) is that of an n-type FET. In this case, the on-state is characterized instead by $V_g > V_{g0}$. With the drain *grounded* and the source with *positive* V_{sd} bias, the *positive* voltage now *decreases* the carrier concentration. The current which flows from source to drain is now given by:

$$I_{sd} = \frac{\mu_e C'_g}{L} \left(V_o - \frac{1}{2} V_{sd} \right) V_{sd}.$$

Notice that the electron mobility μ_e was used instead of μ_h .

We will now define a *field-effect mobility* μ_{FET} from Equation 3.7. This is given by⁴:

$$\mu_{FET} \equiv -\frac{L}{C'_g} \frac{\partial G}{\partial V_g}. \quad (3.8)$$

We see that the mobility is directly proportional to $\partial G/\partial V_g$, a quantity that will be important later. We will introduce explicitly this quantity in the results to come whenever we can.

For completeness, the small-bias approximation (zeroth order) of the conductance can be written simply as:

$$G = \frac{\mu_h C'_g}{L} V_o = -\frac{\partial G}{\partial V_g} V_o. \quad (3.9)$$

As a last note, we will define the experimentally-relevant *transconductance* g_m :

$$g_m \equiv \left. \frac{\partial I_{sd}}{\partial V_g} \right|_{V_{sd}=const.} = -\frac{\mu_h C'_g}{L} V_{sd} = \frac{\partial G}{\partial V_g} V_{sd}. \quad (3.10)$$

This quantity is very important because it describes how the current changes with the gate voltage for a given bias. It can be used to measure the sensitivity of the device to nearby charges – a property desired in chemical and biological sensors.

⁴ Negative sign reflects *holes*. Use $+\partial G/\partial V_g$ for electrons.

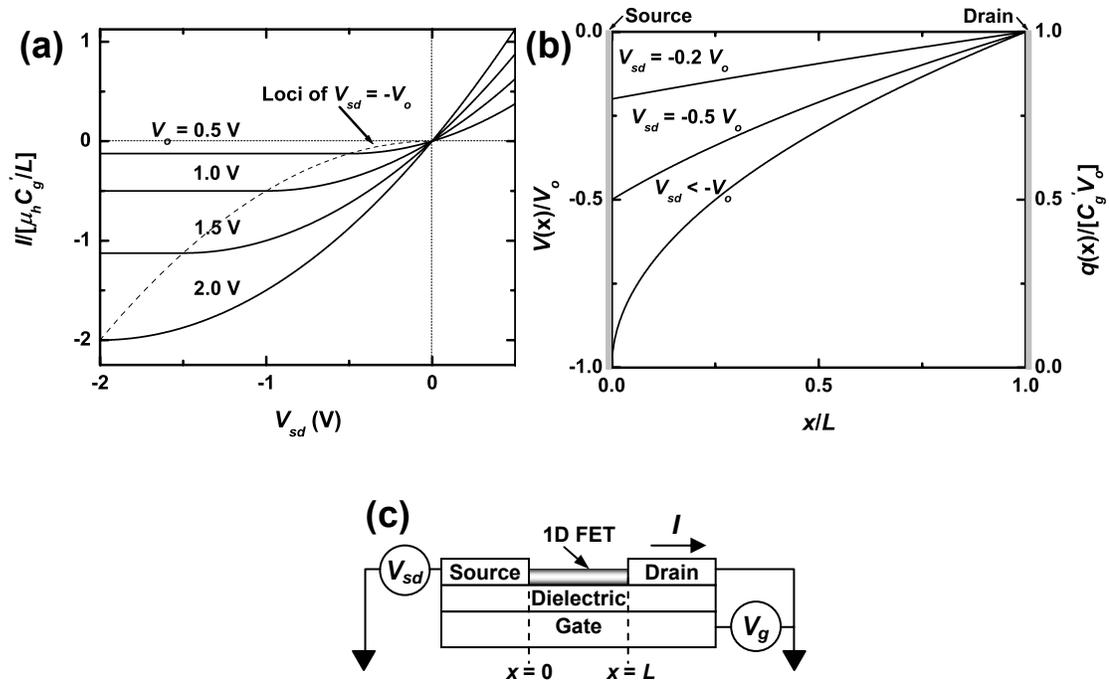


Figure 3.1. Field-effect operation of a 1D-FET. **(a)** Current versus voltage characteristics of a p-type 1D FET according to Equation 3.4. The current first rises linearly (linear region) and then, at negative bias, it becomes constant when $V_{sd} = -V_o$ due to pinch-off, as explained in Section 3.2.2 (saturation region). For low-resistance contacts, the amplitude of the current is calculated once given the mobility, the gate capacitance and the length of the 1D semiconductor. Notice that the current amplitude increases quadratically with the overvoltage in the saturation region. This is the amplification effect which transistors are well-known for. **(b)** Voltage profile along a 1D FET according to Equation 3.5. For low bias, the profile becomes linear. At higher bias, eventually pinch-off happens at the source and the profile becomes approximately constant for $V_{sd} < -V_o$, with a rapid voltage drop at the source end. The right-side axis shows conversely the charge distribution, which is zero at the source when pinch-off happens. Any additional bias results in a local voltage drop at the source end that leaves the voltage profile unchanged in the bulk. **(c)** Schematic of a 1D FET in a typical wire-on-plane gate arrangement, as described in Chapter 2.

3.2.2 Saturation region

Something interesting happens when $V_{sd} = -V_o$, according to Equation 3.2. The carrier concentration at the source end becomes zero. Any attempt at pushing the bias further (more negative) will only expand the extent of the region with zero charge until at some distance x from the source the voltage “drops”⁵ once more to the limit-value $V(x) = -V_o$. This condition is known as *pinch-off*.

Quantitatively, if we set $V(x) = -V_o$ in Equation 3.5, the resulting equation for V_{sd} has only one solution, for $x = 0$ and $V_{sd} = -V_o$. We cannot simply describe the spatial profile of the voltage from the contact until it drops to $-V_o$, since this requires specific knowledge of the depletion region induced in the semiconductor by both gate and source voltages. Nevertheless, if we assume the width of this region $\Delta L \ll L$, we can substitute $V_{sd} = -V_o$ in Equations 3.4, 3.7 and 3.10, and we obtain the current, conductance⁶ and transconductance in the *saturation region*⁷:

$$\begin{aligned}
 I_{sd} &= -\frac{\mu_h C'_g}{L} \frac{(V_o)^2}{2} = \left. \frac{\partial G}{\partial V_g} \right|_{sat} (V_o)^2 \\
 G &= \frac{I_{sd}}{(-V_o)} = \frac{\mu_h C'_g}{L} \frac{V_o}{2} = \left. -\frac{\partial G}{\partial V_g} \right|_{sat} V_o \\
 g_m &= \left. \frac{\partial I_{sd}}{\partial V_g} \right|_{V_{sd}=const.} = \frac{\mu_h C'_g}{L} V_o = -2 \left. \frac{\partial G}{\partial V_g} \right|_{sat} V_o
 \end{aligned} \tag{3.11}$$

⁵ Voltage *drop* will be used in the current context to describe a decrease of the absolute value. The voltage will start negative at the source and end at zero at the grounded drain end, so its magnitude *drops* along the device's length.

⁶ This is the conductance of the *bulk* of the device excluding the pinch-off region. Now V_{sd} becomes the *applied source-drain bias* and the total conductance is simply $G_{total} = I_{sd}/V_{sd}$, with I_{sd} given by Equation 3.11.

⁷ Once pinch-off is reached, the condition $V_{sd} = -V_o$ effectively ties the bias experienced by the bulk semiconductor at the source end to the gate voltage, no matter what the total bias applied to the source is. This has a serious implication to $\partial G/\partial V_g$, which transitions locally from $-\mu_h C'_g/L$ to $-(1/2)\mu_h C'_g/L$ due to the additional modulation of the source bias experienced by the bulk of the device (excluding pinch-off region). The transconductance, on the other hand, retains the same functional form given by Equation 3.10 when going from the linear to the saturation regime.

The voltage profile in the bulk of the 1D semiconductor, obtained from Equation 3.5 with $V_{sd} = -V_o$, is approximately given by:

$$V(x) \cong -V_o \left(1 - \sqrt{x/L}\right), \quad (3.12)$$

where it is assumed that the width of the pinched-off region is $\Delta L \ll L$. This profile predicts a rapid voltage drop at the source end ($V = -V_o/2$ at $x = L/4$) and a gradual profile thereafter. Figure 3.1 parts (a) and (b) also show the saturation region current versus bias characteristics and voltage profile at pinch-off⁸. The saturation region is key for current amplification.

3.2.3 Subthreshold region

At finite temperatures, in the off-region (band gap), a small amount of carriers can be thermally excited even before the threshold voltage V_{g0} is reached. The carrier population is simply given by the Fermi-Dirac distribution $f(E)$ for electrons, $[1-f(E)]$ for holes. The total number of carriers is given by the integration of the density of states times the distribution function. We can instead define an effective density of states at the valence band edge N_v such that the population of holes can be written as (Streetman and Banerjee 2000):

$$\begin{aligned} p_0 &= N_v [1 - f(E_v)] \\ &= N_v \left[1 - \frac{1}{1 + e^{(E_v - E_F)/kT}} \right], \\ &\cong N_v e^{-(E_F - E_v)/kT} \end{aligned} \quad (3.13)$$

⁸ In practical MOSFETs, the length ΔL of the pinch-off region increases proportionally to V_{sd} , to first-order. Since I_{sd} in Equation 3.11 is inversely proportional to the channel length $L - \Delta L$, it can be seen that the saturation current continues to increase as $(1 + (\Delta L/L)V_{sd})$.

where E_v is the valence band energy level, E_F is the Fermi level of the semiconductor, k is the Boltzmann constant and T is the absolute temperature. The approximation in the last line is valid as long as the Fermi level is a few kT above the valence band edge. Thermally excited carriers can then contribute to the current even before the gate threshold is reached by means of the gate voltage V_g .

The relationship between V_g and the energy scale is a function of the electrochemical potentials of the metal plate and the semiconductor and is better characterized by the *subthreshold swing* S , defined as

$$\begin{aligned} S &\equiv \left(d \log I_{sd} / dV_g \right)^{-1} \\ &\approx \ln 10 \cdot \left(d(\text{const.} + (E_v - E_F)/kT) / dV_g \right)^{-1}, \\ &\approx \frac{kT}{\alpha e} \ln 10 \end{aligned} \quad (3.14)$$

where we assumed a simple exponential profile for I_{sd} from Equation 3.13 and that $\Delta E_v = \alpha e \Delta V_g$. The constant α measures how effectively V_g changes E_v . Ideally, $\alpha = 1$ and $S \sim 60$ mV/decade (at room temperature). This subthreshold current is only important for $V_g > V_{g0}$ (p-type FET) and the derivation was performed in the low-bias approximation.

The subthreshold swing is an important parameter for characterizing gate performance in FETs because it quantifies the steepness of the switching response. A sharp transition from off- to on-state makes for high on/off current ratio, and consequently for two very distinct logic states.

3.3 Carbon nanotube field-effect transistor

The model proposed in Section 3.2 assumed little regarding the band structure of a nanotube. The main hidden assumption was that the conductivity increased

linearly with respect to energy/overvoltage. This is a consequence of another assumption, that the hole mobility was a constant. But as we will see next, the band structure of a carbon nanotube limits its maximum conductivity, and the mobility is a function of energy. As seen in Section 2.2, the density of states (DOS) of a carbon nanotube becomes a constant at high energies as a result of a constant velocity at high energies, since $g(E) \sim v^{-1}$ in 1D. We will now see that this implies a cap to the conductivity.

Under biasing conditions, the carrier density is a function of position along the nanotube according to Equation 3.2, and then the wavevector becomes:

$$k(x) = \frac{\pi N}{4L} = \frac{\pi}{4} \cdot \frac{C'_g}{e} \cdot (V_o + V(x)), \quad (3.15)$$

where we used Equation 2.4 and once more we assumed the voltage convention of a p-type FET with positive voltage on the source.

The major consequence of this result is that the carrier velocity, from Equation 2.3, will also be a function of position, and ultimately the phonon scattering rate $\tau^{-1}(x)$ and the phonon mean free path $l(x)$ as well, through the relation $l(x) = v(x)\tau(x)$.

Using Fermi's Golden Rule (Datta 1997), it can be shown that the scattering rate in 1D is proportional to the DOS (Equation 2.5):

$$\begin{aligned} \tau^{-1} &\propto g \propto v^{-1} \\ \Rightarrow v\tau^{-1} &= v_0\tau_0^{-1}, \end{aligned} \quad (3.16)$$

where τ_0^{-1} is the scattering rate at high energies and $v_0 = 8 \times 10^5$ m/s, the Fermi velocity in a carbon nanotube at high energies as introduced in Chapter 2.

Now we define the position-dependent conductivity, following Equation 2.9:

$$\begin{aligned}
 \sigma(x) &= \left(\frac{4e^2}{h} \right) l(x) \\
 &= \left(\frac{4e^2}{h} \right) l_0 \left(\frac{v(x)}{v_0} \right)^2, \\
 &= \sigma_0 \left(\frac{v(x)}{v_0} \right)^2
 \end{aligned} \tag{3.17}$$

where we used Equation 3.16, and σ_0 and l_0 are the high-energy conductivity and mean free path, respectively. The quadratic dependence of the conductivity on the velocity is a general property of 1D systems, as long as Equation 3.16 holds. Also notice that the conductivity is limited by the velocity.

Next, we use specific knowledge of the band structure of a carbon nanotube, Equations 2.3 and 3.15, in order to write:

$$\begin{aligned}
 \left(\frac{v(x)}{v_0} \right)^2 &= \frac{\left(\frac{\hbar k}{m^* v_0} \right)^2}{1 + \left(\frac{\hbar k}{m^* v_0} \right)^2}, \\
 &= \frac{\left(\frac{V_o + V(x)}{a} \right)^2}{1 + \left(\frac{V_o + V(x)}{a} \right)^2},
 \end{aligned} \tag{3.18}$$

where $a = 8e/(3\pi dC_g)$ becomes the relevant voltage scale for transport in the FET.

Now we are ready to calculate the conductance of the nanotube FET. We use 3.3, 3.17 and 3.18 to write:

$$\begin{aligned}
I_{sd} &= -\sigma_0 \cdot \frac{\left(\frac{V_o + V(x)}{a}\right)^2}{1 + \left(\frac{V_o + V(x)}{a}\right)^2} \cdot \frac{\partial V(x)}{\partial x} \\
&= -\sigma_0 a \cdot \frac{\left(\frac{V_o + V(x)}{a}\right)^2}{1 + \left(\frac{V_o + V(x)}{a}\right)^2} \cdot \frac{\partial \left(\frac{V_o + V(x)}{a}\right)}{\partial x}, \tag{3.19}
\end{aligned}$$

where we assumed that V_o is a constant, just as we did in Section 3.2.1 (so spatial variations of the gate voltage profile, specially near the contacts, are neglected).

With a change of variables to $y = [(V_o + V(x))/a]$, the indefinite integral $\int [y^2/(1+y^2)]dy = y - \tan^{-1}y$ (it can be shown by trigonometric substitutions), and the *maximum conductance* defined as $G_0 = \sigma_0/L$, we integrate Equation 3.19 from source ($V(0) = V_{sd}$) to drain ($V(L) = 0$) to eliminate the voltage profile:

$$\begin{aligned}
I_{sd} &= -G_0 a \int_0^L \frac{(y(x))^2}{1 + (y(x))^2} \cdot \frac{\partial(y(x))}{\partial x} dx \\
&= G_0 a \int_{\frac{V_o}{a}}^{\frac{V_o + V_{sd}}{a}} \frac{y^2}{1 + y^2} dy \\
&= G_0 a \left[\left(\frac{V_{sd}}{a}\right) - \left[\tan^{-1}\left(\frac{V_o + V_{sd}}{a}\right) - \tan^{-1}\left(\frac{V_o}{a}\right) \right] \right] \tag{3.20}
\end{aligned}$$

The voltage profile can now be calculated, by integrating from 0 to x on *both* sides (V_{sd} drops to $V(x)$), with the constant I_{sd} now given by 3.20. This leads to a transcendental equation.

We can now directly write down the conductance of the nanotube, just as done in Equation 3.7:

$$G = \frac{I_{sd}}{V_{sd}} = G_0 \left[1 - \frac{\left[\tan^{-1}\left(\frac{V_o + V_{sd}}{a}\right) - \tan^{-1}\left(\frac{V_o}{a}\right) \right]}{\left(\frac{V_{sd}}{a}\right)} \right]. \quad (3.21)$$

We can see from this expression that $G \leq G_0$. Notice that this derivation is for a diffusive nanotube FET ($l(x) \ll L$, Equation 2.9).

3.3.1 Nanotube FET in the saturation regime

Equation 3.20 accurately describes the current in a nanotube FET in the diffusive regime. Saturation and subthreshold operation follow the same treatment of Sections 3.2.2 and 3.2.3. We will now elaborate on the saturation region. Pinch-off still happens at a bias $V_{sd} = -V_o$, as seen from Equation 3.15, but now the current profile leading to this point given by Equation 3.20 differs from Equation 3.4 (the relative agreement depends on the diameter of the nanotube). See Figure 3.2 for more detail.

For the sake of completeness, we present the corresponding current, (bulk) conductance and transconductance in the saturation region for comparison with Equation 3.11:

$$\begin{aligned} I_{sd} &= -G_0 V_o + G_0 a \tan^{-1}(V_o/a) \\ G &= \frac{I_{sd}}{(-V_o)} = G_0 - G_0 \frac{\tan^{-1}(V_o/a)}{(V_o/a)}. \\ g_m &= \left. \frac{\partial I_{sd}}{\partial V_g} \right|_{V_{sd}=\text{const.}} = G_0 \frac{(V_o/a)^2}{1 + (V_o/a)^2}. \end{aligned} \quad (3.22)$$

At large overvoltage ($V_o \gg a$), assuming only one subband, $G = g_m = G_0$. That is, both the conductance and the transconductance have the same maximum value. This result

has a special consequence for the transconductance since it imposes a limit on the maximum rate of current change induced by a gate. Then G_0 characterizes the *ultimate* sensitivity of a nanotube sensor⁹.

3.3.2 Nanotube FET at low bias

Although the main application of a transistor is operation in the saturation regime, other applications can arise from the use of small source-drain bias, especially for high-frequency operation. So now we expand the results of Section 3.3 for low bias.

We start with the source-drain current and the conductance, derived from Equations 3.20 and 3.21:

$$\begin{aligned} I_{sd} &= G_0 \frac{(V_o/a)}{1+(V_o/a)^2} \cdot \frac{1}{a} \cdot \left[V_0 + \frac{1}{1+(V_o/a)^2} V_{sd} \right] V_{sd} \\ G &= G_0 \frac{(V_o/a)^2}{1+(V_o/a)^2} \left[1 + \frac{1}{1+(V_o/a)^2} \left(\frac{V_{sd}}{V_o} \right) \right] \end{aligned} \quad (3.23)$$

The arrangement of the variables in I_{sd} was done so as to facilitate its comparison to Equation 3.4. The source-drain bias “correction” to the overvoltage is now weighed by the factor $[1 + (V_o/a)^2]^{-1}$, which equals $\frac{1}{2}$ when $V_o = a$. The voltage profile can be shown to match exactly that of Equation 3.6 when the expansion of \tan^{-1} is done to first order in V_{sd} .

The zero-order value of the conductance is just:

$$G = G_0 \frac{(V_o/a)^2}{1+(V_o/a)^2}, \quad (3.24)$$

⁹ A *ballistic* nanotube has $G_0 = G_Q = 4e^2/h \sim 155 \mu\text{S}$, which is the ultimate *and ideal* sensitivity of a nanotube sensor, as seen in Section 2.3.

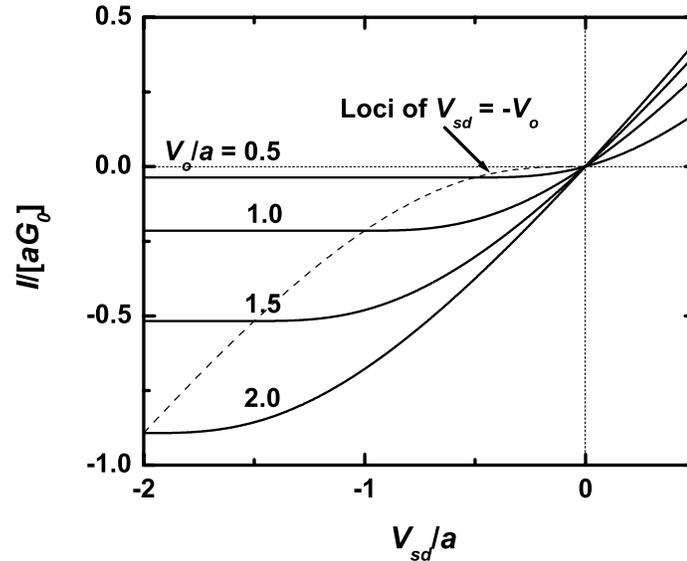


Figure 3.2. Current versus source-drain voltage of a carbon nanotube FET. The current is normalized by the maximum conductance G_0 and the parameter a . This parameter sets a voltage scale which does not exist for the constant-mobility 1D FET. By definition, G_0 depends on the mean-free-path, which can be shown to be proportional to the diameter (Suzuura and Ando 2002; Zhou, Park et al. 2005). The result of this is that the product aG_0 is *nearly* diameter-dependent (a depends on the diameter as well through the gate capacitance, which is a weak function of diameter when the gate plate is placed far from the nanotube's surface). If we use a typical wire-on-plane gate geometry with 200 nm of silicon oxide as the dielectric and the definition of a , we find that $a = 1$ V when the diameter is $d \sim 4$ nm. This converts the horizontal axis in the figure in units of Volts. A smaller diameter results in a larger voltage scale, shifting in turn pinch-off at a given bias voltage towards lower absolute currents. As a consequence, thinner carbon nanotubes should carry less current at the same bias. The diameter can therefore directly modify the I - V characteristics.

showing once more that the conductance has a maximum value G_o ¹⁰. This expression is extremely useful for low-bias measurements. A comparison between the low- and high-bias conductances (along with the corresponding field-effect mobilities, to be discussed next) is shown in Figure 3.3.

3.3.3 Field-effect mobility

Let us study the field-effect mobility of a carbon nanotube FET, as defined in Equation 3.8. It is then straightforward to apply it to Equation 3.24 to obtain the zero-order approximation¹¹:

$$\mu_{FET} = \frac{e\tau_0}{m^*} \frac{(V_o/a)}{(1 + (V_o/a)^2)^2}, \quad (3.25)$$

where the constants a and l_0 were re-expressed in order to show the familiar pre-factor $e\tau_0/m^*$.

Since μ_{FET} is proportional to $\partial G/\partial V_g$, and we know that the conductance stops increasing at large overvoltages, the mobility should have a peak¹². If we set $\partial\mu_{FET}/\partial V_g = 0$ we find:

$$\begin{aligned} (\mu_{FET})_{peak} &= \frac{9}{16\sqrt{3}} \frac{e\tau_0}{m^*} = 0.32 \frac{e\tau_0}{m^*} \\ (V_o)_{peak} &= \frac{a}{\sqrt{3}} = \frac{8e}{3\sqrt{3}\pi d C_g'} \end{aligned} \quad (3.26)$$

¹⁰ Notice that the no-bias conductance of Equations 3.24 and 3.9 have the same functional dependence as the high-bias transconductance of Equations 3.22 and 3.10, respectively. This is because both are independent of V_{sd} and, from the definition of g_m , the derivative with respect to V_g is equivalent to a derivative with respect to V_{sd} in the saturation regime.

¹¹ It is not possible to compare directly Equations 3.4 and 3.23 because it is not clear how to take into account the weighing/averaging factor outside the square brackets.

¹² In contrast, Equation 3.7 has a constant mobility. In reality, the mobility of 3D FETs degrades at higher gate voltages, resulting in a similarly peaked function.

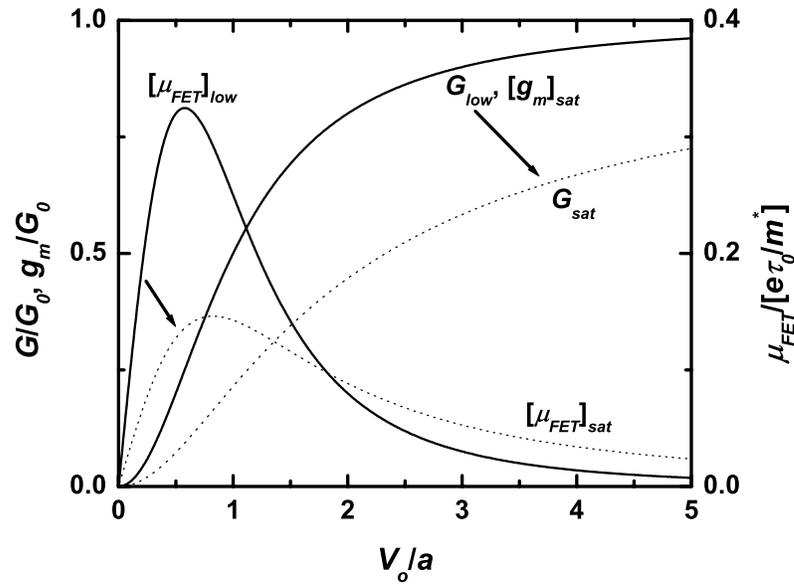


Figure 3.3. Low-bias versus saturation regimes for a carbon nanotube FET. **Left axis:** conductance G and transconductance g_m (saturation transconductance only) versus overvoltage scaled by the device-dependent voltage scale a , according to Equations 3.22 and 3.24. The conductance, defined as the ratio I_{sd}/V_{sd} , increases slowly in the saturation regime (the maximum value is still G_0). The saturation transconductance has the same functional form (and units) as the low-bias conductance. **Right axis:** field-effect mobility versus overvoltage at low bias (Equation 3.25) and in saturation (by differentiation of Equation 3.22 for G). It follows the derivative of the conductance, and as such, it peaks when the conductance change is the steepest. Notice that the peak moves towards larger overvoltage for higher bias. As expected, the mobility goes to zero at low and large overvoltage.

For a nanotube without defects, one could think of using the position of the peak of $\partial G/\partial V_g$ to estimate the tube diameter.

3.4 Simple analysis of effect of the contacts

When the contact resistances at source and drain are comparable to the bulk resistance of the nanotube, the voltage drop at the contacts cannot be neglected anymore. The two conductances we are trying to compare are the contact conductance G_{cs} (both contacts included) and the nanotube conductance G . The total conductance measured in an experiment will be $G_{tot} = (G^{-1} + G_{cs}^{-1})^{-1}$. This will be a function of the bulk conductance of the nanotube if G_{cs} is low and constant¹³ (as a function of V_{sd} and V_g). Typical experimental contact resistances of nanotubes FETs can range from ~ 10 k Ω to M Ω . Bulk resistivities, on the other hand, have been seen in the range 4-20 k $\Omega/\mu\text{m}$ when the nanotubes are in the on-state (Zhou, Park et al. 2005). The magnitudes of the bulk and contact contributions in the on-state are therefore comparable. Contact resistances are typically a very important part of the total on-state conductance.

A prediction can be made regarding how the contacts affect the peak of $\partial G_{tot}/\partial V_g$ when compared to $\partial G/\partial V_g$ of the bulk. The first derivative of the total conductance is:

¹³ The voltage drops at the individual contacts in fact matter, due to their relation to the gate threshold. If the drain resistance is much smaller than the source resistance, the voltage applied to the drain of the nanotube will be at ground, while the one at the source will be lower than V_{sd} by a certain amount. If the source resistance becomes much smaller than the drain resistance, then the nanotube source will be at V_{sd} while the drain will be above ground by a certain amount. Although these situations are irrelevant to a resistor, they are not equivalent when there is a gate capacitor nearby. The induced charge profile, and with it the voltage profile, become distinct. Since we will be concerned mostly with small bias throughout the rest of the chapter, these nuances will be neglected.

$$\frac{\partial G_{tot}}{\partial V_g} = \frac{\partial}{\partial V_g} (G^{-1} + G_{cs}^{-1})^{-1} = \left(\frac{\partial G}{\partial V_g} \right) \left(1 + \frac{G}{G_{cs}} \right)^{-2}, \quad (3.27)$$

where we used that G_{cs} is a constant.

We now set the second derivative to zero to find the peak, from which we obtain the equation:

$$\begin{aligned} \frac{\partial^2 G_{tot}}{\partial V_g^2} = 0 &= \left(1 + \frac{G}{G_{cs}} \right)^{-3} \left[\frac{\partial^2 G}{\partial V_g^2} \left(1 + \frac{G}{G_{cs}} \right) - \frac{2}{G_{cs}} \left(\frac{\partial G}{\partial V_g} \right)^2 \right] \\ \Rightarrow \left(\frac{\partial^2 G}{\partial V_g^2} \right) G / 2 \left(\frac{\partial G}{\partial V_g} \right)^2 &= \left(1 + \frac{G_{cs}}{G} \right)^{-1} \end{aligned} \quad (3.28)$$

Use Equation 3.24 (low-bias conductance) and we end up with the equation:

$$3(1 + \eta_0)x^4 + (3 + 2\eta_0)x^2 - \eta_0 = 0, \quad (3.29)$$

where $\eta_0 = (G_{cs}/G_0)$ and $x = (V_o/a)$. The solution is:

$$(V_o)_{peak} = \frac{a}{\sqrt{3}} \left[1 + \frac{G_0}{G_{cs}} \right]^{-\frac{1}{2}}. \quad (3.30)$$

For low-resistance contacts ($G_{cs} \rightarrow \infty$), we recover Equation 3.26. So we see that the overvoltage for the peak of $\partial G_{tot}/\partial V_g$ to happen is smaller than that of $\partial G/\partial V_g$. This means the conductance becomes steepest at a more positive V_g (smaller overvoltage; see mobility plot of Figure 3.4).

This entire derivation was done in the low-bias regime. It is not possible to obtain an analytical solution to the peak overvoltage including the effect of bias. This

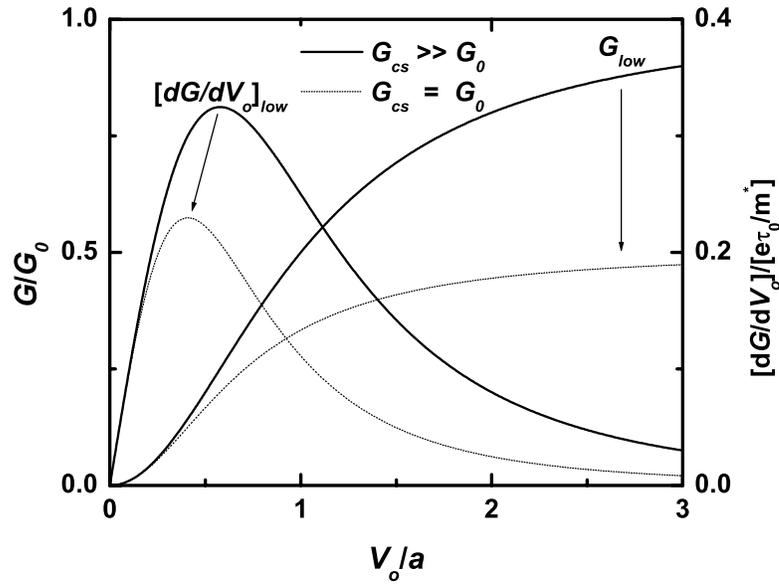


Figure 3.4. Effect of ohmic contacts to the low-bias conductance of a carbon nanotube FET. **Left axis:** low-bias conductance versus overvoltage scaled by parameter a . When the contact resistances increase, the total conductance is limited by the rule $G_{tot} = (G^{-1} + G_{cs}^{-1})^{-1}$, where G is the conductance of the nanotube bulk and G_{cs} is the conductance of the two contacts together. In this particular case, the maximum conductance is $G_0/2$. **Right axis:** scaled derivative of the conductance, or alternately the scaled field-effect mobility. The mobility peaks at lower overvoltages (more positive gate voltages in a p-type FET) when the contacts become more resistive.

will not be a concern, since we will be interested only in the low-bias regime in the following chapters. The importance of $\partial G/\partial V_g$ at high frequencies will be then demonstrated.

3.5 Schottky barrier

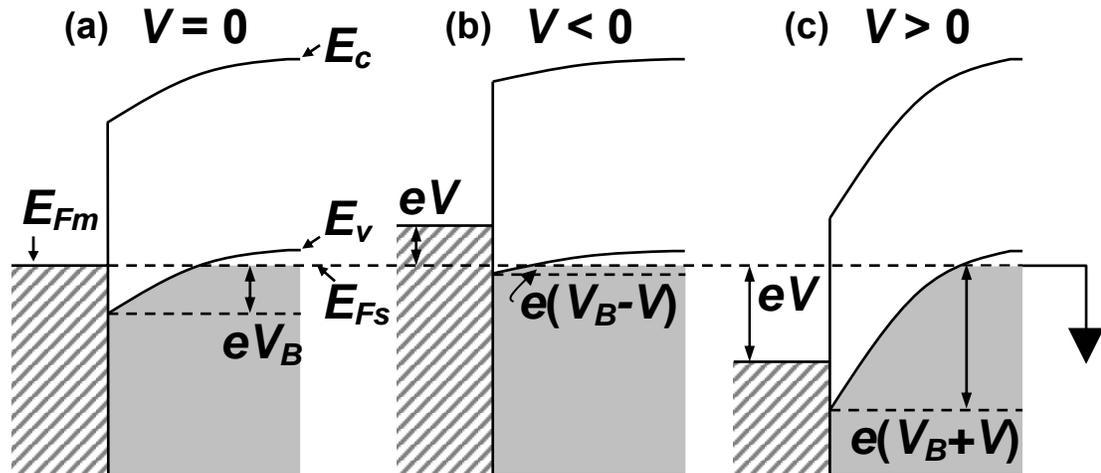
If we put a metal and a nanotube in contact, they exchange charge¹⁴. Let us start with the equilibrium situation (no bias applied), and let us assume that the nanotube (the semiconductor) is grounded by means of an ohmic contact with low resistance. In equilibrium, the Fermi level of the metal and the nanotube must align. Charge equilibration, on the other hand, modifies the shape of the bands near the interface. Precisely at the interface, the work function mismatch is translated into a built-in potential. Furthermore, as argued in Chapter 1, carbon nanotubes are typically heavily p-doped and their Fermi level should be found below the valence band edge at zero gate voltage. This is the situation in the bulk of the nanotube.

The mismatch between the chemical potentials of the metal and the nanotube can result in two different outcomes, as shown in Figure 3.5 (a) through (c) and (d). For a p-type contact¹⁵, when the Fermi level of the metal pins into the valence band of the semiconductor at the interface, there will be no barrier for holes – the majority carriers in the nanotube – to move from the metal to the nanotube. This is an *ohmic* contact (part (d); see Yaish, Park et al. 2004 and Javey, Guo et al. 2003). Otherwise, if the metal pins the interface with Fermi level inside the band gap, there will be a barrier, called a *Schottky* barrier (Heinze, Tersoff et al. 2002; Heinze, Radosavljevic et al. 2003).

¹⁴ This happens differently from the MOS capacitor, where charge cannot flow directly from the gate to the semiconductor. In this case, the voltage drops along the interface in the materials (no dielectric). In fact, since the density of states in the nanotube (away from band edge) is orders of magnitude lower than that in the Fermi sea of the metal, the voltage drop happens almost entirely in the nanotube.

¹⁵ All the rules discussed here for holes are also true for electrons in n-type semiconductors, with the appropriate considerations applied. These can be found in standard device physics textbooks.

Schottky



Ohmic

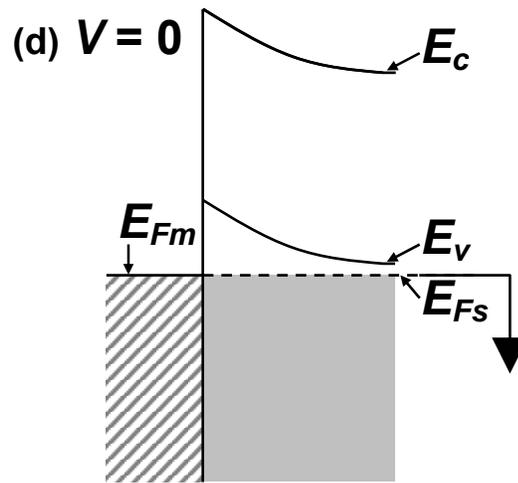


Figure 3.5. Types of metal-nanotube contacts. Schottky barriers – (a) At zero bias, the Fermi levels E_{Fm} (metal) and E_{Fs} (nanotube) align. The work function difference establishes a built-in potential barrier V_B for holes to flow from the metal to the nanotube (assumed heavily p-doped and grounded at the opposite contact) and vice-versa. (b) Negative bias applied to the metal decreases the potential barrier from the nanotube to the metal to $V_B - V$. (c) Barrier increases when bias is positive. Notice that the barrier from the metal to the nanotube remains at V_B . Furthermore, the electrical potential is constant in the metal. The metal-nanotube junction behaves like a reverse-biased diode. (d) An ohmic contact has low resistance and does not change with bias. In the figure, there is no barrier for transport either way.

Under applied bias, the ohmic contact will immediately conduct. The Schottky contact, on the other hand, will have a barrier height that depends on the sign of the applied bias. The rules for biasing the Schottky junction are given as follows. Assume the nanotube is kept grounded by an ohmic contact not shown in the figure. At zero bias, the energy barrier for diffusion of holes from the nanotube to the metal is measured as eV_B from the top of the valence band at the junction to the Fermi level of the nanotube (part (a)). When a *negative* bias voltage V is applied to the metal, it draws holes towards the interface of the nanotube. The Fermi level of the metal is raised relative to its original grounded position by an energy eV (and so are the valence and conduction bands at the interface). The barrier for holes in the nanotube is lowered (part (b)) to $e(V_B - V)$. Notice a tendency for the bands to become flattened spatially. Finally, if a *positive* bias voltage V is applied to the metal, holes are depleted from the nanotube. Now the barrier for holes in the nanotube increases (part (c)) to $e(V_B + V)$.

The energy barrier for holes moving from the metal to the nanotube is eV_B at all times, despite the bias. This means that the hole current flowing into the nanotube provides an offset to the opposing hole current flowing into the metal, even when the latter is negligible, such as for large positive bias. This is a reverse current similar to the one in p-n junction diodes. Although the details are somewhat different, the current through a Schottky contact has the same functional form of the current of a diode:

$$I = I_{Sat} (e^{\alpha V} - 1), \quad (3.31)$$

where I_{Sat} is the reverse saturation current and α determines the voltage scale over which the device behaves nonlinearly. The convention used for the voltage V and the

current I is the same as that of a p-n junction, with the nanotube as the p-type semiconductor.

3.6 Conclusions

In this chapter, we have developed the theory of dc conductance of carbon nanotube FETs at both low and high biases. We started by assuming a constant mobility, similar to the analytical treatment of a standard MOSFET. Later, we relaxed this assumption by taking into consideration the band structure of a 1D material (carbon nanotube). Although we did an entirely dc analysis, these properties will be of fundamental importance in understanding the high-frequency behavior of carbon nanotube FETs. This will be the scope of the next chapter.

CHAPTER 4

MIXING THEORY OF CARBON NANOTUBES

4.1 Introduction

As seen in Chapter 2, a carbon nanotube's electrical properties are determined by its resistance, capacitance and inductance. In dc measurements, the resistance of the nanotube is finite, while the capacitive reactance to ground of the gate is infinite ($X_C = [\omega C]^{-1}$) and the series inductive reactance is zero ($X_L = \omega L$). This picture must change in the ac regime. At high enough frequencies, ac current flows to the gate (for $\omega > [RC]^{-1}$), and the inductance increases the series ac impedance (for $\omega > R/L$). In particular, when the series resistance is negligible, we obtain a standard lossless transmission line (characteristic impedance $Z_0 = [L/C]^{1/2}$ (Pozar 1998)). This would be the case of a ballistic nanotube, for example. Such a nanotube transmission line would have a wave velocity dominated by the kinetic inductance, as defined in Chapter 2.

A direct measurement of the high-frequency properties of a carbon nanotube consists of transmitting a signal down the device and measuring the output at the same frequency of the input. This is challenging due to the high impedance of a nanotube (as seen in Chapter 2, $R_{min} = R_Q = 6.45 \text{ k}\Omega$) when compared to the impedance of typical measurement equipment (50Ω). Any transmitted signals become too small and difficult to detect (poor signal-to-noise-ratio).

Indirect measurements, on the other hand, involve the use of nonlinear effects. Semiconducting nanotubes, in particular, present themselves with an intrinsic nonlinearity: a gate-controlled resistivity. It happens that nonlinearities such as the field-effect from the gate or Schottky contacts also add to the ac response by means of an effect called *frequency mixing*, or *mixing* for short. This can be observed at low

frequencies, which makes for detection that is within reach of standard experimental equipment. This is in contrast with direct measurements, which necessitate specialized high-frequency equipment. Mixing is therefore a technique to measure the high-frequency response of a device. But the nature of this technique also makes it a probe of the device's nonlinear characteristics, a welcome bonus feature.

In this chapter, we will introduce the theory of mixing and apply it to carbon nanotube field-effect transistors (FETs). For most of the discussion, the nanotube will be treated as a single mixing unit. At the end of this chapter, we will model mixing of a carbon nanotube in the RC limit of a transmission line, much resembling a very lossy cable. Using this model, we will make predictions about the frequency response of mixing. We will then use this model in Chapter 7 to analyze mixing from semiconducting nanotubes in the diffusive regime.

4.2 General theory of mixing

The current produced by a bias applied to a diode or transistor will generally be a nonlinear function of the same applied bias¹. For a small modulation δV applied to a pre-existing constant bias V_{sd} , we can simply express this current as an infinite series:

$$I_{sd}(V_{sd} + \delta V) = I_{sd}(V_{sd}) + \left. \frac{\partial I_{sd}}{\partial V} \right|_{V=V_{sd}} \cdot \delta V + \left. \frac{\partial^2 I_{sd}}{\partial V^2} \right|_{V=V_{sd}} \cdot \frac{(\delta V)^2}{2} + \dots \quad (4.1)$$

¹ For a transistor, the nonlinearity comes from the gate response.

If we set $V_{sd} = 0$, further simplifications are possible²:

$$I_{sd}(\delta V) = \left. \frac{\partial I_{sd}}{\partial V} \right|_{V=0} \cdot \delta V + \left. \frac{\partial^2 I_{sd}}{\partial V^2} \right|_{V=0} \cdot \frac{(\delta V)^2}{2} + \dots = G \delta V + \left. \frac{\partial G}{\partial V} \right|_{V=0} \cdot \frac{(\delta V)^2}{2} + \dots, \quad (4.2)$$

where $G = (\partial I_{sd} / \partial V)|_{V=0}$ is the low-bias conductance.

If this modulation is additionally time-dependent, of the form $\delta V = V_{ac} \cos(\omega t)$, and neglecting higher-order terms, we obtain:

$$\begin{aligned} I_{sd}(V_{ac}, \omega) &= G V_{ac} \cos(\omega t) + \left. \frac{\partial G}{\partial V} \right|_{V=0} \cdot \frac{V_{ac}^2}{2} \cdot \cos^2(\omega t) \\ &= \left(\frac{1}{4} \left. \frac{\partial G}{\partial V} \right|_{V=0} \cdot V_{ac}^2 \right) + (G V_{ac}) \cdot \cos(\omega t) + \left(\frac{1}{4} \left. \frac{\partial G}{\partial V} \right|_{V=0} \cdot V_{ac}^2 \right) \cdot \cos(2\omega t) \end{aligned}, \quad (4.3)$$

where the terms were arranged in order of the harmonics of the frequency ω . In obtaining the last line, we used the trigonometric relation $\cos^2(\omega t) = \frac{1}{2}(1 + \cos(2\omega t))$.

What is remarkable about the last result is that although the input oscillates at a fixed frequency ω , the output also contains a dc and a 2ω component (if the whole series were used, all harmonics of the fundamental would appear). The dc component corresponds to *rectification* and is directly related to the high-frequency properties of the device, since V_{ac} is the amplitude of the input at ω and $\partial G / \partial V$ might be ω -dependent. We will refer to this as the *dc mixing current* I_{mix} ³:

² Without bias, $I_{sd}(0) = 0$.

³ The term mixing refers to generating an output of linear combinations of the input frequencies. In this case, ω mixes with itself by means of the power of 2, producing the frequencies $\omega \pm \omega$. Something similar can be done with an amplitude modulated (AM) input as well. In this case, $\delta V = V_{ac} \cdot (1 + m \cdot \cos(\omega_m t)) \cdot \cos(\omega_c t)$, where ω_m is the modulation frequency, ω_c is the carrier frequency (typically higher than ω_m) and m is the modulation index. Because $\cos(\omega_m t) \cdot \cos(\omega_c t) = \frac{1}{2}(\cos((\omega_c - \omega_m)t) + \cos((\omega_c + \omega_m)t))$, we will see already in first order an output current at the lower frequency $\omega_c - \omega_m$, and in second order the even lower $\omega_c - 2\omega_m$, and so on. By tuning the frequency difference, we can use this frequency mixing to perform ac detection at reasonably low frequencies, improving signal-to-noise ratio related to 1/f noise.

$$I_{mix}(V_{ac}, \omega) \equiv \frac{1}{4} \frac{\partial G(\omega)}{\partial V} V_{ac}^2, \quad (4.4)$$

where we inserted a possible frequency dependence of $\partial G/\partial V$. It should be noted that this derivative should be evaluated in the zero-bias limit whenever it appears from now on. This current provides means of measuring the high-frequency properties of a device by performing dc detection, which is easy to implement experimentally⁴.

A few special cases will now be analyzed.

4.2.1 The Schottky diode

A biased Schottky junction such as that described in Chapter 3 (Equation 3.31) will output a current of the form⁵:

$$I = I_{Sat} (e^{\alpha V} - 1), \quad (4.5)$$

where V is the voltage difference between the metal and the semiconductor. The convention is such that forward current flows from the metal to an n-type material or from a p-type material to the metal. The constant α is the inverse of the voltage scale over which the device is nonlinear, and it equals e/kT for an ideal diode. The current I_{Sat} is the *reverse saturation* current ($I \rightarrow -I_{Sat}$ for negative V). See Streetman (Streetman and Banerjee 2000) for more.

⁴ Without going into details, a special case can happen with an FET. If the conductance of the device is tuned by a gate voltage V_g , then the application of a modulation $\delta V_g = V_{g,ac} \cos(\omega_g t)$ to the gate will make $G \rightarrow (\partial G/\partial V_g) \delta V_g$ to first order in δV_g . Then, the first-order term in δV in Equation 4.3 will generate mixing of the two input frequencies (output will contain $\omega \pm \omega_g$). This kind of control is particularly useful when the device is suspended, in which case mechanical vibrations can be set to resonate at a high frequency ω , with the driving force given by the gate's electrostatic tunable pull.

⁵ This corresponds to the metal-semiconductor contact of Chapter 3. Such a contact can also be thought of as a p-n junction with the metal behaving as a p⁺ contact or n⁺ (+ denotes high doping), depending on the relative majority carrier sign.

Using the expansion of Equation 4.3 for small bias, we obtain:

$$I = I_S \left(\alpha V + \frac{1}{2} \alpha^2 V^2 \right) = \frac{V}{R_{j0}} + \frac{1}{2\alpha R_{j0}} (\alpha V)^2, \quad (4.6)$$

where $R_{j0} = (I_{Sat}\alpha)^{-1}$ is the zero-bias *junction resistance* (by definition, $R_j = (\partial I/\partial V)^{-1}$).

We can directly extract the dc mixing current from Equation 4.4 by time-averaging the second-order term of Equation 4.6:

$$I_{mix}(V_{ac}, \omega) = \frac{1}{4} I_{Sat} (\alpha V_{ac})^2 = \frac{\alpha}{4R_{j0}} V_{ac}^2. \quad (4.7)$$

The frequency dependence may exist in I_{Sat} , R_{j0} or α . We will soon return to the subject of Schottky barrier mixing with carbon nanotubes in this chapter.

4.2.2 Mixing with an FET

An FET will output a dc mixing current from Equation 4.4 given by the binomial expansion of the current, Equation 3.4 of Chapter 3:

$$I_{mix}(V_{ac}, \omega) = \frac{1}{4} \frac{\mu_h C'_g}{L} V_{ac}^2 = -\frac{1}{4} \frac{\partial G(\omega)}{\partial V_g} V_{ac}^2, \quad (4.8)$$

where we have included phenomenologically a frequency dependence in the conductance. Comparison with Equation 4.4 shows that we have simply replaced $\partial G/\partial V$ with $-\partial G/\partial V_g$. This can be understood qualitatively from Equation 3.2 of Chapter 3. A *positive* $\delta V(x)$ *increases* the local charge distribution in the same manner

that a *negative* δV_g does, in the limit of low-resistance contacts. Thus follows $\partial G/\partial V = -\partial G/\partial V_g$ ^{6,7}.

4.3 Theoretical mixing with a nanotube FET

With this reasoning in mind, we can write down the expected dc mixing current of a nanotube FET, using Equation 4.8 and Equation 3.25 of Chapter 3:

$$I_{mix}(V_{ac}, \omega) = -\frac{1}{4} \frac{\partial G(\omega)}{\partial V_g} V_{ac}^2 = -\frac{1}{4} \left[-\frac{e\tau_0}{m^*} \frac{(V_o/a)}{(1+(V_o/a)^2)^2} \frac{C'_g}{L} \right]_{\omega} V_{ac}^2. \quad (4.9)$$

The immediate consequence is that this mixing current should exhibit all the interesting properties of the mobility as described in Chapter 3. It should peak as a function of gate voltage and tail off to zero at large enough overvoltage.

4.4 Contact resistances and Schottky mixing

Real devices have contact resistances, and these could affect mixing. As discussed in Chapter 3, the contacts can be either ohmic or Schottky. Ohmic contacts do not generate any mixing current and can be introduced as constant resistances in addition to the resistance of the nanotube. Their main role is in attenuating the mixing current I_{mix} as follows. We take the nanotube mixer shown in Figure 4.1 as consisting of a dc current source $I_{mix,bulk}$ in parallel with the resistance R of the bulk of the nanotube. Although the dc current source is a result of the high-frequency nonlinearity, the dc current flowing through the entire circuit depends on the resistance of the dc

⁶ In contrast, a positive $\delta V(x)$ decreases the local charge distribution in the same manner that a negative δV_g does for an n-type FET, as seen in Equation 3.2 of Chapter 3. Again it follows that $\partial G/\partial V = -\partial G/\partial V_g$, and Equation 4.8, remarkably, is valid for both n and p-type FETs.

⁷ This equality is only valid in the limit of low-resistance contacts. It fails when the voltage drop is split among bulk and contacts.

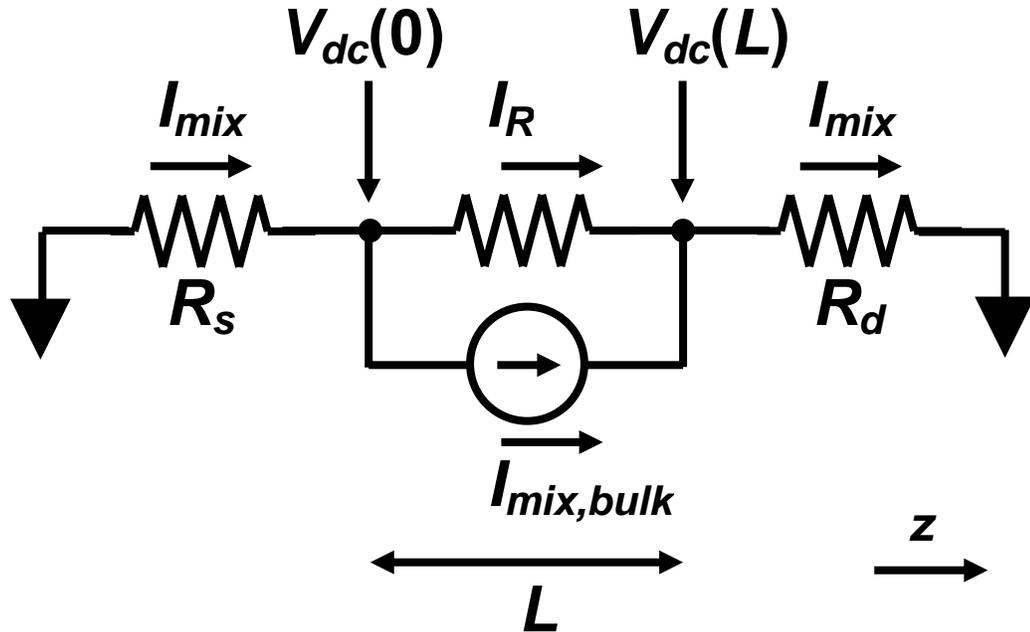


Figure 4.1. Nanotube dc mixer model with constant contacts. $I_{mix,bulk}$ is the ac-generated mixing current of the nanotube mixer of length L . A dc voltage $V_{dc}(z)$ builds up across the device in order to keep the total mixing current at each node constant and equal to I_{mix} . The dc current that builds up across the resistance R of the device is given by $I_R = [V_{dc}(z=0) - V_{dc}(z=L)]/R$. The resistances of the source and drain are R_s and R_d , respectively. The dc boundary condition in this case is that source and drain are grounded.

path. If the ends are grounded and the contacts do not mix, a dc voltage $V_{dc}(z)$ will build up across the bulk of the nanotube to compensate for the excess mixing current generated.

Using Kirchhoff's current law at the nodes/contacts under the condition of grounded ends, the total mixing current measured becomes:

$$I_{mix} = I_{mix,bulk} + \frac{V_{dc}(0) - V_{dc}(L)}{R} = \frac{0 - V_{dc}(0)}{R_s} = \frac{V_{dc}(L) - 0}{R_d}, \quad (4.10)$$

$$\Rightarrow I_{mix} = I_{mix,bulk} \frac{R}{R_{tot}}$$

where the bulk of the nanotube extends from $z = 0$ at the source end to $z = L$ at the drain end, R_s and R_d are the resistances of the source and drain contacts, respectively, and $R_{tot} = R_s + R + R_d$. This shows that the contacts behave as a current divider. This rule should be used whenever dc mixing current appears *in the bulk*.

Now let us calculate Schottky mixing as a function of frequency in the special case of a highly conductive nanotube. This can be used to describe either a metallic nanotube or a semiconducting nanotube at high overvoltage (on-state), as long as the resistances of the contacts are much larger than that of the bulk of the nanotube⁸. The circuit model is shown in Figure 4.2. We label the ac voltage at the source $V_{in} = V_{sd}$, the drain is grounded, and the ac voltage on the nanotube is V_{out} . We assume the low-bias approximation, in which case the junction resistances can be approximated by

⁸ Any model of mixing using the voltage drop along the nanotube at high frequencies has to take into account the distributed resistances and capacitances of the bulk. As a limiting case, when the resistances of the contacts are much larger than that of the bulk, the voltage drop on the nanotube becomes negligible, and we can represent it simply as a capacitor to ground in a small-signal ac model. We will analyze the complete mixing problem in the next section.

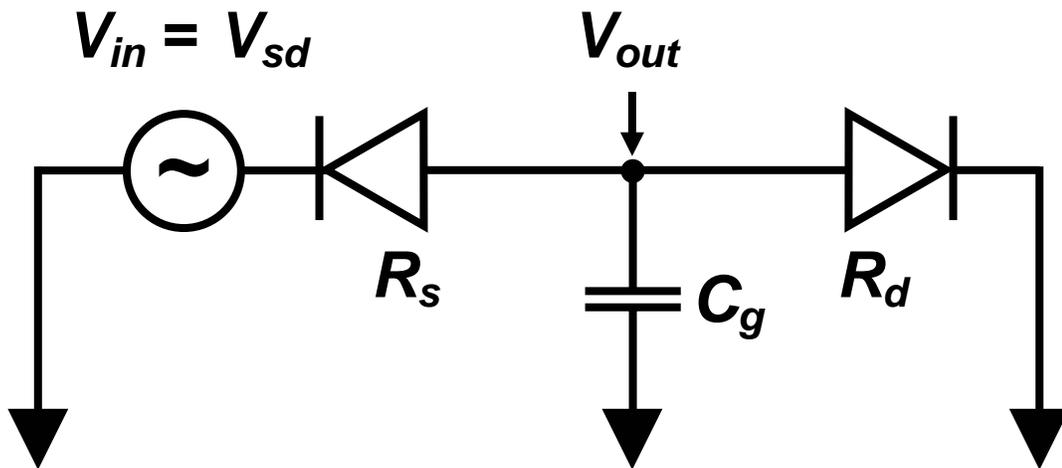


Figure 4.2. Schottky mixer model at ac, in the limit of negligible nanotube resistance. The source and drain contacts are represented by reverse-biased diodes with junction resistances R_s and R_d , respectively. The ac voltage V_{out} is assumed to be uniform in the nanotube. The voltage drops across each contact depend on how the input ac voltage $V_{in} = V_{sd}$ divides.

their bias-independent values R_s (reverse-biased diode) at the source and R_d (forward-biased diode) at the drain¹⁰ (see Equation 4.6).

In the ac picture, both the drain resistance R_d and the gate capacitor C_g are seen as impedances in parallel connected to ground. The voltage gain is simply given by the impedance ratio of $R_d \parallel C_g$ (“ \parallel ” denotes equivalent parallel impedance, between the resistance and the capacitive impedance in this particular case) and the total impedance to ground:

$$\begin{aligned}
 \frac{V_{out}}{V_{in}} &= \frac{R_d \parallel C_g}{R_s + R_d \parallel C_g} \\
 &= \frac{(R_d^{-1} + j\omega C_g)^{-1}}{R_s + (R_d^{-1} + j\omega C_g)^{-1}}, \quad (4.11) \\
 &= \left[(1 + R_s/R_d) + j\omega R_s C_g \right]^{-1} \\
 &= (1 + R_s/R_d)^{-1} \cdot \left[1 + j\omega (R_s \parallel R_d) C_g \right]^{-1}
 \end{aligned}$$

where j is the imaginary constant (engineering notation).

The voltage drop across R_s normalized by V_{in} follows:

$$\frac{V_{in} - V_{out}}{V_{in}} = \frac{-R_s/R_d}{1 + R_s/R_d} \cdot \frac{1 + j\omega R_d C_g}{1 + j\omega (R_s \parallel R_d) C_g}. \quad (4.12)$$

We have been dealing with complex notation so far. The mixing current, though, actually depends on the in-phase component of V^2 , so that in our notation, we change the V^2 dependence of Equation 4.4 by $|V|^2$ (a definite proof for this will be given at the end of this chapter). Then, we should take into account that the Schottky diodes depicted in Figure 4.2 point in opposite directions, and therefore they generate

¹⁰ As discussed in Chapter 3, a carbon nanotube typically operates as a p-type FET. Forward biasing occurs when the voltage on the nanotube is higher than the voltage on the metal.

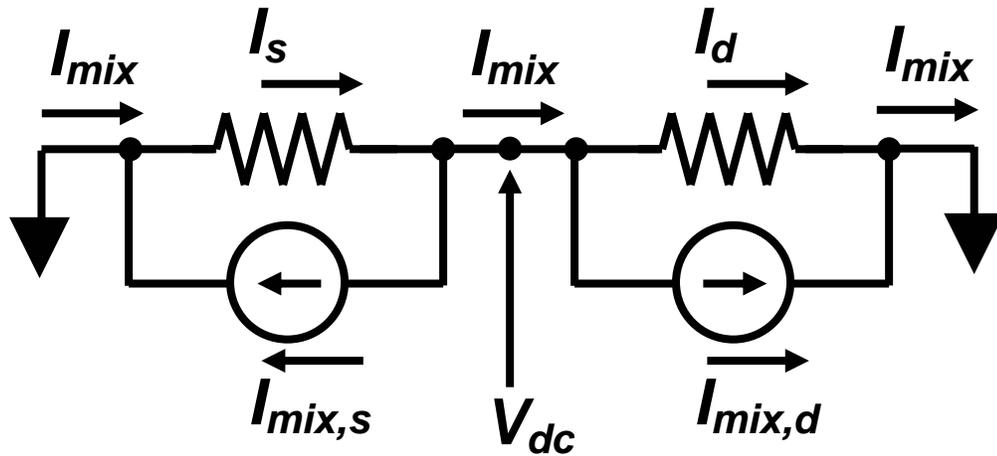


Figure 4.3. Schottky mixer model at dc, in the limit of negligible nanotube resistance. $I_{mix,s}$ and $I_{mix,d}$ are the ac-generated mixing currents of the source and drain Schottky diodes, respectively. A dc voltage V_{dc} builds up in the nanotube in order to keep the total mixing current I_{mix} constant at each node. The dc currents that build up across each contact are given by $I_s = -V_{dc}/R_s$ at the source and $I_d = V_{dc}/R_d$ at the drain. The dc boundary condition is that source and drain are grounded.

mixing currents of opposite sign following Equation 4.7. Figure 4.3 shows how the current divides in this case, and using Equations 4.11 and 4.12 we obtain:

$$\begin{aligned}
I_{mix} &= -I_{mix,s} - \frac{V_{dc}}{R_s} = I_{mix,d} + \frac{V_{dc}}{R_d} \\
\Rightarrow I_{mix} &= \frac{1}{R_{tot}} (-R_s I_{mix,s} + R_d I_{mix,d}) \\
&= \frac{1}{4R_{tot}} \left(-\alpha_s |V_{in} - V_{out}|^2 + \alpha_d |V_{out}|^2 \right) , \\
&= \frac{|V_{in}|^2}{4R_{tot}^3} \frac{[-\alpha_s R_s^2 \cdot (1 + \omega^2 R_d^2 C_g^2) + \alpha_d R_d^2]}{1 + \omega^2 (R_s \parallel R_d)^2 C_g^2}
\end{aligned} \tag{4.13}$$

where the dc voltage that builds up on the nanotube is V_{dc} , the sign of the mixing current of the first contact reflects its polarity (reverse), and $R_{tot} = R_s + R_d$. In order to extract useful predictions from this expression, we will assume that $\alpha_s \sim \alpha_d = \alpha$, so that both contacts have the same nonlinear voltage range. In this case, we convert into the following expression:

$$I_{mix} = \frac{|\alpha V_{in}|^2}{4\alpha} \cdot \frac{(R_d - R_s)}{R_{tot}^2} \cdot \frac{[1 + \omega^2 C_g^2 R_s^2 R_d^2 (R_s^2 - R_d^2)^{-1}]}{1 + \omega^2 C_g^2 (R_s \parallel R_d)^2} . \tag{4.14}$$

One part of this expression looks familiar. The ω -dependent denominator indicates a low-pass RC filter cutoff at a frequency ω_{RC} given by C_g and the equivalent resistance of the contacts in parallel.

Apart from the cutoff, we can identify (see Figure 4.4):

- a) For $R_s > R_d$, $I_{mix} < 0$.
- b) For $R_d > R_s$, $I_{mix} > 0$ at low frequencies; $I_{mix} < 0$ when :

$$\begin{aligned}
1 + \omega^2 C_g^2 R_s^2 R_d^2 (R_s^2 - R_d^2)^{-1} &< 0 \\
\Rightarrow \omega > \omega_{flip} &= \frac{1}{R_s C_g} \sqrt{1 - \left(\frac{R_s}{R_d}\right)^2}.
\end{aligned} \tag{4.15}$$

For $R_d \gg R_s$, $\omega_{flip} = (R_s C_g)^{-1}$. In this limit, $\omega_{RC} = [(R_s || R_d) \cdot C_g]^{-1} = (R_s C_g)^{-1} \cdot (1 + R_s / R_d) \rightarrow (R_s C_g)^{-1}$ as well. In fact, it can be seen that $\omega_{RC} \geq \omega_{flip}$ from these expressions. Approaching the limit $R_s \rightarrow R_d$, we find that even if $R_s / R_d \sim 0.1$, then $\omega_{RC} \sim 1.1 \omega_{flip} \sim (R_s C_g)^{-1}$. It is then hard to tell them apart experimentally, except when $R_d \sim R_s$, when the sign change happens at zero frequency. Our typical experimental values of contact resistances range from $\sim 10 \text{ k}\Omega$ to $\text{M}\Omega$, so for highly asymmetrical barriers, $\omega_{flip} \sim \omega_{RC}$.

- c) In terms of the junction resistance ratio $\eta = (R_s / R_d)$ and the reverse saturation currents $I_{Sat,s}$ and $I_{Sat,d}$ of each contact:

$$\begin{aligned}
\omega = 0, I_{mix} &= \begin{cases} -\frac{I_{Sat,s}}{4} |\alpha V_{in}|^2, & \eta \gg 1 \\ 0, & \eta = 1 \\ \frac{I_{Sat,d}}{4} |\alpha V_{in}|^2, & \eta \ll 1. \end{cases} \\
\omega \gg \omega_{RC}, I_{mix} &= -\frac{1}{4\alpha R_{tot}} |\alpha V_{in}|^2
\end{aligned} \tag{4.16}$$

In summary: at low frequencies, the larger Schottky resistance dominates mixing (and its current polarity). At large enough frequencies, the capacitor shorts the source diode to ground and mixing eventually becomes entirely dominated by the source Schottky diode, resulting in negative current because it is reverse-biased. Its magnitude, however, still depends on the current division rules and can be influenced by the opposite contact (through R_{tot}).

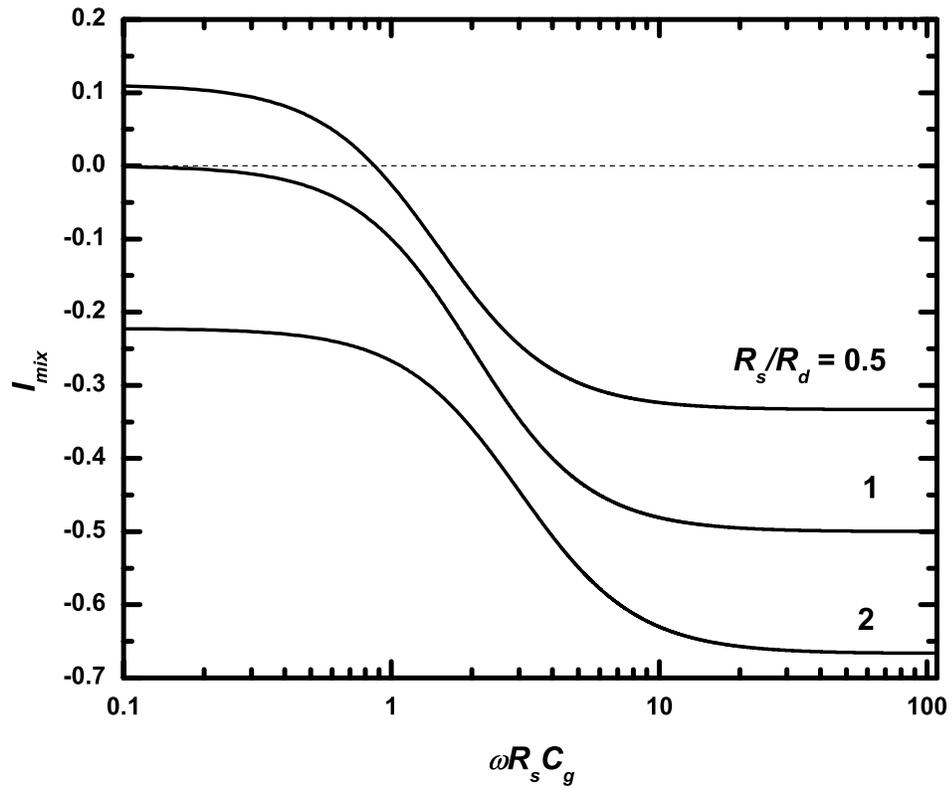


Figure 4.4. Schottky mixing current I_{mix} versus frequency for constant source junction resistance R_s , different drain junction resistances R_d . The current is displayed in units of $|\alpha V_{in}|^2 I_{Sat,s}/4$ and the frequency is normalized by $[R_s C_g]^{-1}$. The constant α is assumed to be the same for both contacts. The current is always dominated by the source diode at high frequencies, acquiring a negative sign.

Notice that a Schottky mixer is essentially a resistor. In the absence of parasitic capacitances at the contacts, Figure 4.4 predicts that the gate capacitor simply regulates which of the two mixers has control over the dc mixing current. The cutoff frequency ω_{RC} in effect cuts off the drain diode from the mixer circuit. As long as the input voltage V_{in} is a constant as a function of frequency, the Schottky mixing current should have constant values on either side of the cutoff.

4.5 Mixing of a nanotube as a lossy transmission line

So far, we have modeled mixing from discrete elements, such as a Schottky diode or an FET as a single mixing component. The former allowed us to predict the frequency-dependence of the mixing current of the contacts of a nanotube when the resistance of the nanotube is negligible (previous section). The latter allowed us to treat a nanotube as a single mixer, despite its distributed resistance and capacitance. Because of this, no inherent cutoffs were predicted for the bulk of the nanotube, and it appeared as if the nanotube mixer could work at indefinitely high frequencies (frequency dependence was implied only in $\partial G/\partial V_g$, Section 4.2.2). The question then becomes: if we take into account the distributed nature of the nanotube, will there be any cutoffs?

4.5.1 Carbon nanotube as a transmission line

We start by deriving wave propagation in an FET transmission line in the low-bias limit, using a distributed circuit model. In this treatment, as shown in Figure 4.5, the line can be represented by a series of discrete (length Δz) resistances intercalated by capacitors connected to a ground line.

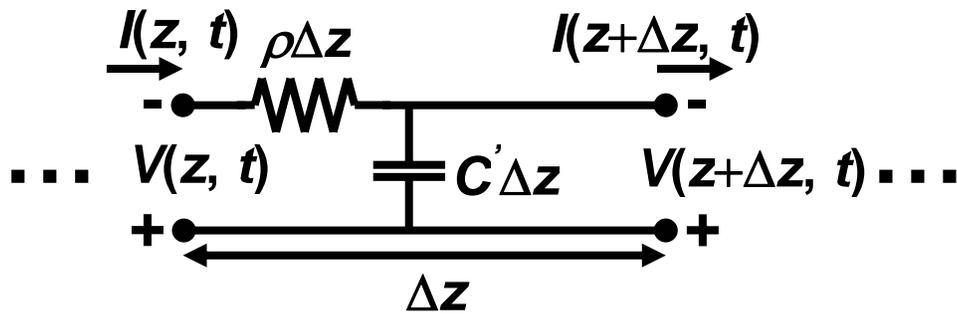


Figure 4.5. Lossy transmission line model. The ac voltage and current profiles are functions of the resistivity and capacitance per unit length of the line. In the text, we use a discrete element of length Δz to derive the profiles. For a typical nanotube resistivity (in the on-state) of $\sim 10 \text{ k}\Omega/\mu\text{m}$, and with the kinetic inductance $L'_{K0} \sim 4 \text{ nH}/\mu\text{m}$ (see Chapter 2), the inductive reactance only becomes comparable to the nanotube's resistance at a frequency $f \sim \rho/(2\pi L'_{K0}) \sim 400 \text{ GHz}$. We cannot access this regime with our experimental equipment. For this reason, we will consider solely the RC limit in our analysis.

Kirchhoff's voltage law gives us:

$$\begin{aligned} V(z + \Delta z, t) &= V(z, t) - \rho(z)\Delta z I(z, t) \\ \Rightarrow \sigma(z)\frac{\partial V(z, t)}{\partial z} &= -I(z, t) \end{aligned} \quad , \quad (4.17)$$

where $\rho(z) = \sigma^{-1}(z) = G^{-1}(z)/\Delta z$ is the average value of the resistivity within the discrete element, and we divided both sides by Δz and took the limit in order to write the last line.

Kirchhoff's current law gives us:

$$\begin{aligned} I(z + \Delta z, t) &= I(z, t) - C' \Delta z \frac{\partial V(z, t)}{\partial t} \\ \Rightarrow \frac{\partial I(z, t)}{\partial z} &= -C' \frac{\partial V(z, t)}{\partial t} \end{aligned} \quad , \quad (4.18)$$

where $C' = C/L$ is the capacitance per unit length to ground (which is also the gate capacitance), and once more we took the limit $\Delta z \rightarrow 0$.

Next, for a sinusoidal steady-state condition such that $V(z, t) = V(z)\exp(j\omega t)$ and $I(z, t) = I(z)\exp(j\omega t)$, the two equations become:

$$\begin{cases} I(z) = -\sigma(z)\frac{\partial V(z)}{\partial z} \\ \frac{\partial I(z)}{\partial z} = -j\omega C' V(z) \end{cases} \quad . \quad (4.19)$$

We can now eliminate the current from these equations by differentiating the first one with respect to z . By use of Equations 3.2 and 3.3 of Chapter 3, we re-express $\sigma(z) = n(z)e\mu = \mu C'(V_o + V(z))$, and we obtain:

$$\frac{\partial}{\partial z} \left[(V_o + V(z)) \frac{\partial V(z)}{\partial z} \right] = \left(\frac{j\omega}{\mu} \right) V(z). \quad (4.20)$$

This leads to a non-ordinary second-order differential equation. Instead of solving the general-bias case, we focus on our region of interest, of low-bias. Then, $V(z) \ll V_o$, and the resistivity $\rho = (\mu C' V_o)^{-1}$ becomes a constant as a function of bias. Our differential equation reduces to:

$$\frac{\partial^2 V(z)}{\partial z^2} = \left(\frac{j\omega}{\mu V_o} \right) V(z) = j\omega \rho C' V(z), \quad (4.21)$$

with solution

$$V(z) = V_+(0)e^{-\gamma z} + V_-(0)e^{\gamma z} = V_+(z) + V_-(z), \quad (4.22)$$

where the *propagation constant* is $\gamma = [j\omega \rho C']^{1/2} = (1+j)\gamma_0$ (real and imaginary parts equal to $\gamma_0 = [\omega \rho C' / 2]^{1/2}$). It then also follows, from Equation 4.19, that:

$$\begin{aligned} I(z) &= I_+(0)e^{-\gamma z} + I_-(0)e^{\gamma z} = I_+(z) + I_-(z) \\ &= \frac{\gamma}{\rho} [V_+(0)e^{-\gamma z} - V_-(0)e^{\gamma z}] \end{aligned} \quad (4.23)$$

from which we can define the *characteristic impedance* Z_0 of the lossy line as:

$$Z_0 = \frac{V_+(z)}{I_+(z)} = -\frac{V_-(z)}{I_-(z)} = \frac{\rho}{\gamma} = \sqrt{\frac{\rho}{j\omega C'}} = (1-j) \frac{\rho}{\sqrt{2\omega \rho C'}}, \quad (4.24)$$

which represents the geometrical mean of the resistance and the capacitive impedance. We see that this impedance is very high at low frequencies ($\omega RC \ll 1$).

We will now analyze the voltage profile along a nanotube. In order to avoid Schottky mixing, we will develop a model that corresponds to a semiconducting nanotube in linear gate operation at low overvoltage¹¹. We will label the source and drain resistances R_s and R_d , respectively. Figure 4.6 corresponds to the schematic of the nanotube transmission line.

The starting point is to find the input impedance of our line. We must analyze the line from the drain end back to the source for this. The drain resistance is a load terminated in ground, and we use it to define a reflection coefficient Γ of the drain:

$$\begin{aligned} R_d &= \frac{V(L)}{I(L)} = Z_0 \frac{V_+(L) + V_-(L)}{V_+(L) - V_-(L)} \\ \Rightarrow \Gamma(L) &= \frac{V_-(L)}{V_+(L)} = \frac{V_-(0)e^{\gamma L}}{V_+(0)e^{-\gamma L}} = \Gamma(0)e^{2\gamma L} = \frac{R_d - Z_0}{R_d + Z_0} \end{aligned} \quad (4.25)$$

In the limit of either negligible drain resistance or low frequency, $\Gamma(L) \rightarrow -1$.

Following the same reasoning, we calculate the input impedance Z_{in} :

$$\begin{aligned} Z_{in} &= \frac{V(0)}{I(0)} = Z_0 \frac{V_+(0) + V_-(0)}{V_+(0) - V_-(0)} = Z_0 \frac{1 + \Gamma(0)}{1 - \Gamma(0)} \\ &\rightarrow Z_0 \frac{1 - e^{-2\gamma L}}{1 + e^{-2\gamma L}} = Z_0 \tanh(\gamma L) \quad , R_d \ll Z_0 \end{aligned} \quad (4.26)$$

In the low-frequency limit, the last line reduces to $Z_{in} \rightarrow R$, where R is the resistance of the bulk of the nanotube.

¹¹ At higher overvoltage, we cannot neglect the mixing contributions of the contact resistances. Although we will not develop the complete theory including the effect of Schottky contacts, it is straightforward to implement it from the analysis that will be presented. Once the ac voltage profile is deduced, we can calculate the amount of Schottky mixing from Equation 4.7. Then we use the rules of current division, in a similar fashion to Equation 4.10, to calculate the total dc mixing current.

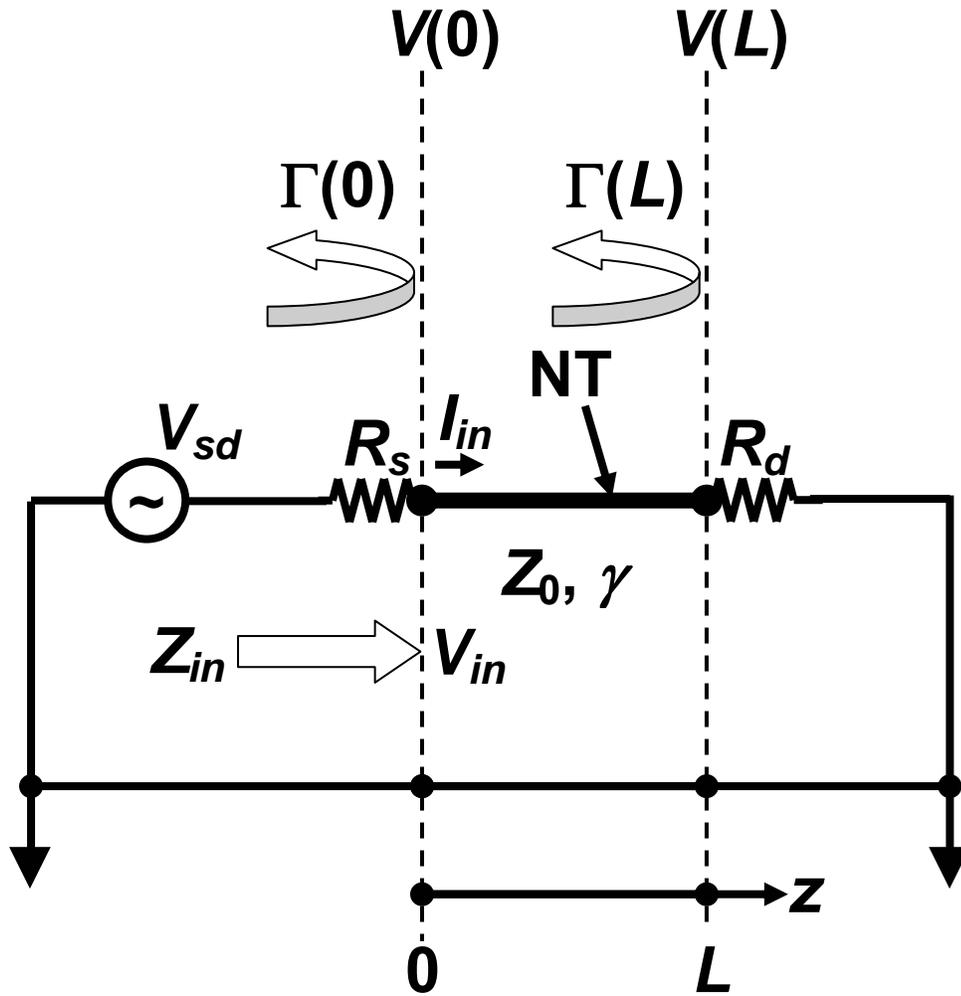


Figure 4.6. Transmission line circuit for nanotube (NT) with contacts. The contact resistances are R_s and R_d for the source and drain, respectively. The input impedance, current and voltage are Z_{in} , I_{in} and V_{in} , respectively; the characteristic impedance and the propagation constant of the nanotube are Z_0 and γ , respectively. All the quantities above have been defined in the text.

Next, we apply our boundary conditions to the input. If the ac input has an amplitude V_{sd} , the voltage seen by the nanotube at $z = 0$ is given by an impedance ratio:

$$V(0) = V_{sd} \frac{Z_{in}}{Z_{in} + R_s}. \quad (4.27)$$

In the limit of negligible source resistance¹², $V(0) \rightarrow V_{sd}$.

Finally, the voltage profile becomes:

$$\begin{aligned} V(z) &= V_+(0) \left(e^{-\gamma z} + \Gamma(0) e^{\gamma z} \right) \\ &\rightarrow V_{sd} \frac{\sinh[\gamma(L-z)]}{\sinh(\gamma L)}, \quad R_d \ll Z_0, R_s \ll Z_{in}. \end{aligned} \quad (4.28)$$

In the low-frequency limit the last line reduces to

$$V(z) = V_{sd} (1 - z/L), \quad (4.29)$$

which is simply a linear profile with no imaginary part, just as we would expect.

Notice that this result was obtained for negligible contact resistances. When contacts are included, the profile is still linear, but the total voltage drop is reduced from V_{sd} .

4.5.2 Mixing with an FET transmission line

So far, these results are analogous to the treatment of a lossy cable (or a metallic nanotube in the diffusive regime). If the line is in fact a transistor (semiconducting nanotube), the *local* current is given by the microscopic Ohm's law

¹² A typical ac source has an internal impedance of 50 Ω . A matched circuit has the same input impedance, which maximizes the amount of power delivered to the load. Here, we neglect the internal impedance of the generator compared to the typically much higher contact resistances and bulk impedance of the nanotube.

from Equation 3.3 of Chapter 3. The local dc mixing current is given by the local dc time-averaged current¹³, which assuming only harmonic fields (Jackson 1975) is:

$$\begin{aligned}
I_{mix}(z) &= \langle \sigma(z, t) E(z, t) \rangle = \left\langle \frac{1}{4} [\sigma(z) e^{-j\omega t} + \sigma^*(z) e^{j\omega t}] \cdot [E(z) e^{-j\omega t} + E^*(z) e^{j\omega t}] \right\rangle \\
&= \left\langle \frac{1}{2} \text{Re} [\sigma^*(z) E(z) + \sigma(z) E(z) e^{-2j\omega t}] \right\rangle = \frac{1}{2} \text{Re} [\sigma^*(z) E(z)] \\
\Rightarrow I_{mix}(z) &= \mu_h C'_g \left\langle (V_o + V(z, t)) \left(-\frac{\partial V(z, t)}{\partial z} \right) \right\rangle \\
&= \frac{1}{2} \mu_h C'_g \text{Re} \left[V^*(z) \left(-\frac{\partial V(z)}{\partial z} \right) \right] = -\frac{1}{2} \frac{\partial G}{\partial V_g} L \text{Re} \left[V^*(z) \left(-\frac{\partial V(z)}{\partial z} \right) \right]
\end{aligned} \tag{4.30}$$

where we used the relation between the field-effect mobility and the derivative $\partial G/\partial V_g$ from Section 3.3.3 of Chapter 3¹⁴. This derivation is general and also applies to Schottky mixing, as seen in Section 4.4. In fact, this is the analytical proof of the treatment we employed then¹⁵.

This local ac nonlinearity gives us a dc current. What we need to know next is how the local dc mixing current produces the total dc mixing current. In the dc picture, the nanotube mixer can be represented as a series of components given by the local resistance in a range Δz and a *current source* in parallel¹⁶, just as done when analyzing the contacts in Section 4.4. The dc current, given by Equation 4.30, is generated by the ac mixer at each point. A dc voltage can build up across each of the parallel resistances, producing another dc current. According to Kirchhoff's current law, these

¹³ To look at the time-average at another frequency ω , multiply by $\exp(j\omega t)$ and take average. If the conductivity and the field have each one frequency component only at ω , the only other averaging possibility is 2ω . Notice that an additive constant (such as V_o) averages to zero.

¹⁴ The local mixing expression is the same in the low-bias limit for the nanotube FET of Section 3.3 of Chapter 3. We use Equation 3.19 and expand the denominator for low bias in first order in $V(z)$ (very important step). The derivation is tedious and will not be displayed here.

¹⁵ Although the Schottky contact is not a distributed mixer, the mixing current (neglecting sign and dc attenuation) is calculated as $I_{mix} = \langle G(t) \Delta V(t) \rangle \sim |\Delta V|^2$, at low bias. This proves our previous statement.

¹⁶ The capacitances look just like infinite impedances to ground in the dc picture. But they should be taken into account for current mixing detection other than the dc. In that case, the lumped resistance should be replaced with the appropriate lumped impedance.

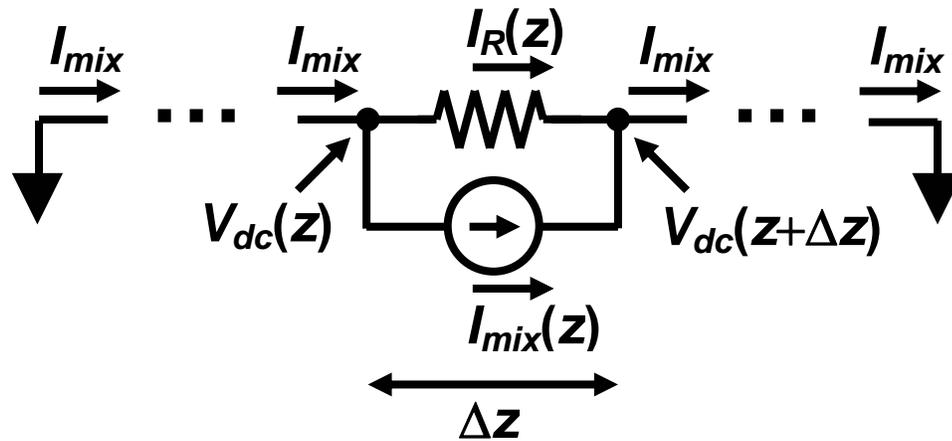


Figure 4.7. Distributed dc mixer model. $I_{mix}(z)$ is the ac-generated mixing current at each point, for each discrete element of length Δz . A dc voltage $V_{dc}(z)$ builds up across the device in order to keep the total mixing current at each node constant and equal to I_{mix} . The dc current that builds up across the resistance of the device is given locally by $I_R(z) = -\Delta V_{dc}(z)/\rho\Delta z$. The boundary condition in this particular case is that source and drain are grounded.

parallel currents add up to a constant at each node (see Figure 4.7) which must be equal to the total dc mixing current at the end. *In the absence of contact resistances*, we can write:

$$I_{mix} = I_{mix}(z) - \frac{\Delta V_{dc}(z)}{\rho \Delta z}, \quad (4.31)$$

where $\Delta V_{dc}(z) = V_{dc}(z+\Delta z) - V_{dc}(z)$ corresponds to the dc voltage difference which builds up locally, and the resistivity was assumed constant again (low-bias limit). The boundary conditions on the dc voltage will be such that the nanotube is grounded at both ends. In that case, when we integrate both sides of this equation along the whole length of the nanotube, we obtain:

$$I_{mix} = \int_0^L I_{mix}(z) \frac{dz}{L}. \quad (4.32)$$

The dc voltage drops out because of the boundary conditions¹⁷. If the dc bias is not zero, the total current becomes offset by the dc current. Notice that after calculating the mixing current, we can re-insert it into this Equation and integrate for $z < L$ to compute the dc voltage profile.

¹⁷ *General solution*: if Schottky contacts are included and the device is grounded at both ends, we obtain:

$$\begin{aligned} I_{mix} &= I_{mix}(z) - \frac{\Delta V_{dc}}{\rho \Delta z} = -\frac{V_{dc}(0)}{R_s} - I_{mix,s} = \frac{V_{dc}(L)}{R_d} + I_{mix,d} \\ \Rightarrow I_{mix} &= \frac{1}{R_{tot}} \left(-R_s I_{mix,s} + R \int_0^L I_{mix}(z) \frac{dz}{L} + R_d I_{mix,d} \right) \end{aligned}$$

where R is the resistance of the bulk of the nanotube, and the signs of the Schottky currents from source and drain are those adopted in Section 4.4.

In the case of low-resistance contacts, we use Equation 4.28 to calculate I_{mix} :

$$\begin{aligned}
I_{mix} &= -\frac{1}{2} \frac{\partial G}{\partial V_g} \int_0^L \text{Re} \left[V^*(z) \left(-\frac{\partial V(z)}{\partial z} \right) \right] dz \\
&= \left[-\frac{1}{4} \frac{\partial G}{\partial V_g} V_{sd}^2 \right] \frac{2\gamma_0 \int_0^L \{ \sinh[2\gamma_0(L-z)] + \sin[2\gamma_0(L-z)] \} dz}{\cosh(2\gamma_0 L) - \cos(2\gamma_0 L)}. \quad (4.33) \\
&= -\frac{1}{4} \frac{\partial G}{\partial V_g} V_{sd}^2 !!!
\end{aligned}$$

Several algebraic steps were omitted in this calculation (including all manipulation with complex numbers and hyperbolic function algebra), but the final result is that the mixing amplitude is independent of frequency and identical to Equations 4.8 and 4.9. The core assumptions were low bias, and non-mixing and low-resistance contacts. If we choose to take into account the dc attenuation from the non-mixing contacts, we simply insert this result into Equation 4.10.

We can calculate the dc bias that builds up in this situation (low-resistance contacts):

$$\frac{V_{dc}(z)}{RI_{mix}} = \left[\frac{\cosh[2\gamma_0 L(1-z/L)] - \cos[2\gamma_0 L(1-z/L)]}{\cosh(2\gamma_0 L) - \cos(2\gamma_0 L)} \right] - \left(1 - \frac{z}{L} \right), \quad (4.34)$$

where $R = \rho L$ is the total resistance of the nanotube bulk and I_{mix} is the same as 4.33.

This result is plotted in Figure 4.8 (a). It shows that below a cutoff of $\omega \sim RC$ the voltage profile is parabolic, as is expected from a low-frequency expansion of the equation above. At high frequency, the dc field (derivative of the potential) is extremely strong near the source. If we compare it with the local mixing current as given by Equation 4.30 (part (b)), we see that the mixing current is highly

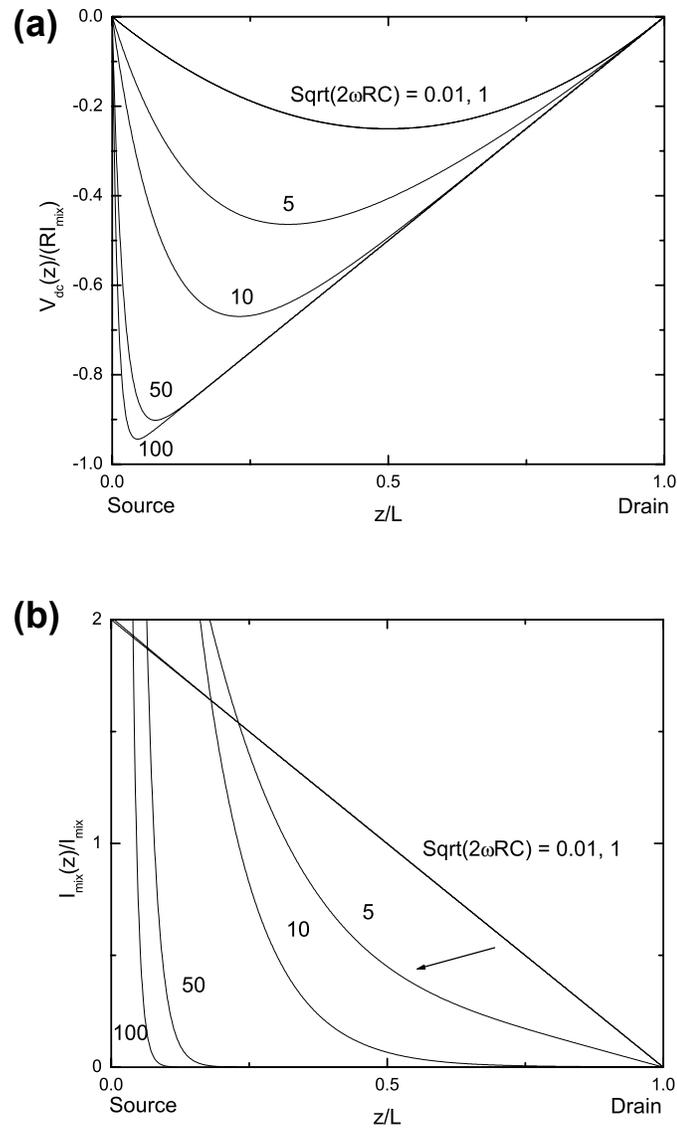


Figure 4.8. Build-up of dc voltage in a 1D distributed mixer. **(a)** Theoretical dc voltage profile (normalized by $R \cdot I_{mix}$) that builds up in a nanotube due to mixing, in the limit of negligible contact resistances. Until $\omega \sim RC$, the voltage profile is homogeneous. Beyond that, a strong dc field ($-\partial V_{dc}/\partial z$) develops at the source. The local mixing current profile, as shown in **(b)** normalized by the total dc mixing current, also becomes larger at the source at these frequencies.

concentrated at the source as well, at high frequencies. The dc voltage that builds up has to provide for an opposing dc current that keeps the total dc mixing current constant. Hence the sign of the dc potential is negative and decreasing. If the mixing current locally falls below the total mixing current, the local dc potential must then increase in order to provide the remaining current.

In spite of the apparent dependence of the built-up dc voltage profile on the RC constant of the bulk of the nanotube, its distributed-circuit nature results in no cutoff of the dc mixing current in the limit of low contact resistances. At high frequencies, when contact resistances are taken into account, the ac current is shunted to ground through the gate and the ac voltage at the source end of the nanotube has a cutoff given roughly by the contact resistance of the source and the gate capacitance. The full ac solution can be constructed from Equations through 4.28 for finite source and drain resistances. In the limit of high-resistance contacts with a low-resistance nanotube, we would obtain the same ac voltage drop at the (constant) source contact as that given by Equation 4.11 in Section 4.4. Using Equation 4.27:

$$\begin{aligned} \frac{V(0)}{V_{sd}} &= \frac{R_d \parallel C_g}{R_s + R_d \parallel C_g} \\ &= (1 + R_s/R_d)^{-1} \cdot [1 + j\omega(R_s \parallel R_d)C_g]^{-1} \end{aligned} \quad (4.35)$$

The cutoff frequency is again given by the resistance of the contacts in parallel and the gate capacitance. This ac voltage attenuation directly affects the amplitude of the mixing current.

In taking into account the contacts with a nanotube mixer, we will first look at mixing in the special case of $R_d \rightarrow 0$. We use Equations , 4.33 and 4.10 to obtain¹⁸:

¹⁸ Equation 4.10 introduces the extra factor of R/R_{tot} which takes care of the dc current division.

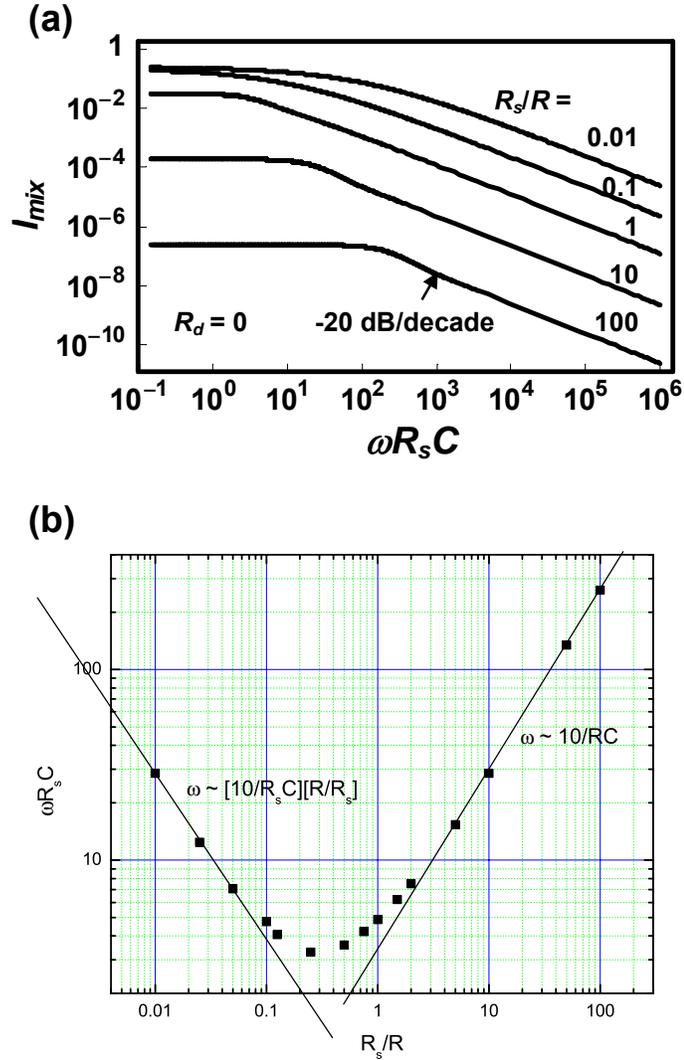


Figure 4.9. Model of dc mixing current of a nanotube distributed mixer in the limit of negligible drain resistance. **(a)** Mixing current in units of $|V_{sd}|^2 \cdot (-\partial G/\partial V_g)$ plotted against normalized frequency $\omega R_s C$. As the nanotube device becomes more conductive, the ratio R_s/R and the overall attenuation increase. For a given trace, the cutoff frequency is measured at the point that I_{mix} drops to half of its dc value, and it is plotted in **(b)**. For $R_s < R$, the cutoff *decreases* as the resistance of the bulk of the nanotube. For $R_s > R$, it *increases* as the inverse of the resistance of the bulk. The turning point is located at $R \sim 4R_s$. At high frequencies there is a constant slope of 20 dB/decade (for voltage), corresponding to one simple low-pass filter. Notice that the cutoff frequency is *never* below $(R_s C)^{-1}$.

$$I_{mix} = -\frac{1}{4} \frac{\partial G}{\partial V_g} V_{sd}^2 \left| \frac{Z_0 \tanh(\gamma L)}{Z_0 \tanh(\gamma L) + R_s} \right|^2 \left(\frac{R}{R + R_s} \right). \quad (4.36)$$

This mixing current normalized by $|V_{sd}|^2 \cdot (-\partial G/\partial V_g)$ is plotted versus $\omega R_s C$ for several values of the ratio R_s/R , Figure 4.9. In the frequency plot, we see a strange theoretical trend: the cutoff frequency (defined for $I_{mix}(\omega) = \frac{1}{2} I_{mix}(\omega = 0)$) decreases as the nanotube bulk becomes more conductive in part (a) (increasing overvoltage) and eventually increases again in part (b). The high-frequency limit of mixing has always a slope of 20 dB/decade for voltage¹⁹ (one factor of 10 drop in I_{mix} per factor of 10 increase in frequency), as expected for a first-order low-pass filter. In part (c), we plot the cutoff frequency against the ratio R_s/R . As we pointed out already, we can see the decreasing/increasing trends of the cutoff. The turning point is approximately located at $R_s \sim R/4$. The approximate frequency asymptotes versus R_s/R show that indeed the cutoff frequency is proportional to the resistance of the nanotube when the bulk is in a resistive state, and is inversely proportional to the resistance when the bulk is in a conductive state. The cutoff frequency is *never* below $(R_s C)^{-1}$.

The exact model with the drain contact included can also be analyzed graphically, but the analytical derivation is cumbersome and the whole expression will not be shown (see more details in Appendix). Instead, we display a few plots of the theoretical frequency dependence of mixing with the drain contact included, Figure 4.10. The mixing current is once more shown normalized by $|V_{sd}|^2 \cdot (-\partial G/\partial V_g)$ and plotted versus $\omega R_s C$. In order to detect the analytical trends, we will analyze simultaneously the following plots: $R_s = 0.1 R_d$ (part (a)), $R_s = R_d$ (part (b)) and $R_s = 10 R_d$ (part (c)).

¹⁹ 1 dB = -10 Log₁₀($A/A_{reference}$), where A is power or some other related intensity. Since $I_{mix} \sim |V|^2$, a drop of one order of magnitude in current corresponds to 10 dB for mixing, or 20 dB for voltage amplitude. We will choose to use the voltage as a reference, since it is one of the typical standards.

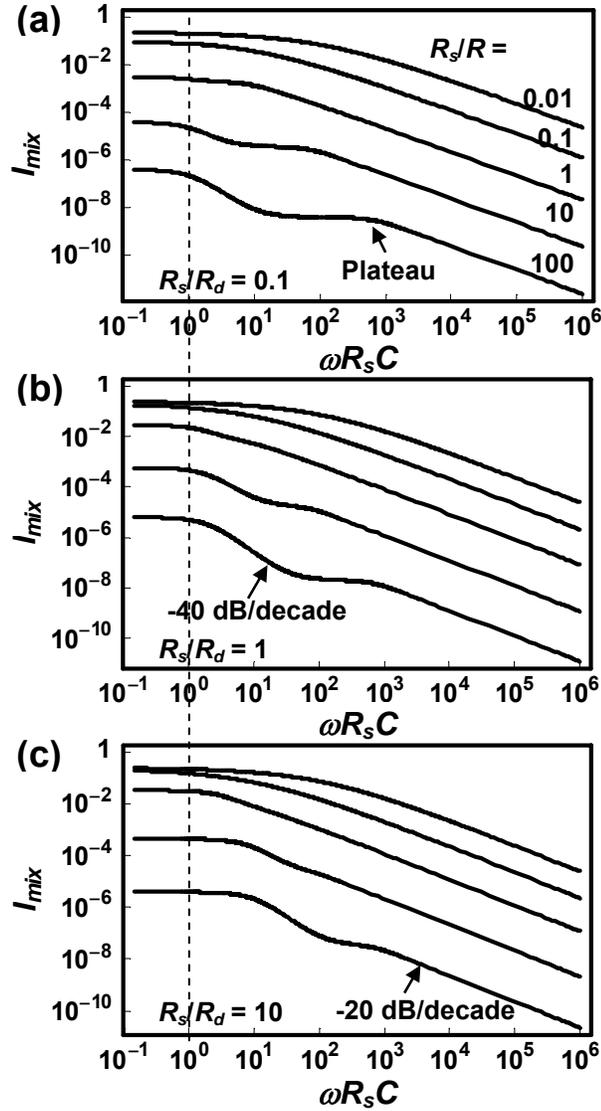


Figure 4.10. Current I_{mix} at dc in units of $|V_{sd}|^2 \cdot (-\partial G / \partial V_g)$ plotted against normalized frequency $\omega R_s C$, model with contacts included. The ratio of source resistance R_s to drain resistance R_d is 0.1, 1 and 10 for parts (a), (b) and (c), respectively. As the nanotube device becomes more conductive, the ratio R_s/R and the overall attenuation increase. Cutoffs are evident. For $R_s < R$, the cutoff decreases as the resistance of the nanotube bulk, similarly to Figure 4.9. For $R_s > R$, more than one cutoff develops. If we concentrate in a range $10 > R_s/R > 0.1$, only one cutoff is more pronounced. The high-frequency slope is 20 dB/decade (for voltage), corresponding to one simple low-pass filter. Also notice that the cutoff frequency is *never* below $(R_s C)^{-1}$. Other features are mentioned in the text.

Roughly, for $R_s \leq R$ the cutoff frequency decreases proportionately to R , just as in the case of $R_d = 0$ which we just analyzed using Equation . For $R_s \geq R$, on the other hand, we detect more than one roll-off for voltage: a brief, low-frequency 40 dB/decade roll-off and a 20 dB/decade roll-off at high frequency. A plateau develops in between the two when $R_s \gg R$. This physically corresponds to low-pass filters which selectively turn on/off as a function of frequency. The sudden sharp slope at low frequency corresponds to two filters cascaded in series. Both appear to turn on and off simultaneously. The high-frequency roll-off, on the other hand, has the slope of a single low-pass filter. Let us explain this behavior in terms of the resistances involved.

In all cases in which $R_s \geq R$, the first frequency cutoff appears to move as R_s in parallel with R_d , just as predicted by Equation 4.35. The smaller of the two contact resistances will therefore impose the lower limit on the cutoff frequency. As the resistance of the device decreases further, the cutoff moves to higher frequencies, as in Figure 4.9. In a real device, however, the contact resistances are typically within a factor of 10 from each other. This justifies looking at the roll-off in the range presented ($10R_d > R_s > 0.1 R_d$)²⁰.

Finally, we conjecture that there is a competition for the attenuation of the average electrical potential on the nanotube (mostly coming from the source contact) and of the potential difference across it (dominated by the drain contact), both essential parameters for mixing (see Equation 4.30). This should account for the sharp slopes at low frequency and the plateaus. But once more, in a real device, the contact resistances and the nanotube bulk resistance are also typically within a factor of 10 from each other. This justifies analyzing this range only ($10R > R_s > 0.1 R$), which corresponds to the three inner traces in Figures 4.10, parts (a), (b) and (c). In all of

²⁰ Also notice that, as seen in Chapter 3, the conductance of a real nanotube FET is ultimately limited by the constant carrier velocity at large overvoltages. If the contact resistances are constant with respect to gate voltage, then once the bulk resistance of the nanotube stops decreasing, the cutoff frequency should become a constant as well (as long as contacts do not mix).

these, there appears to be only one cutoff frequency; the other effects are barely noticeable. From the plots, the lower limit of the cutoff is that from the source contact (this corresponds to a resistance lower than the source resistance, since $\omega < R_s C$). The high-frequency 20 dB/decade slope is once more expected because in this limit the ac current flows to the gate and the attenuation is dominated by the source contact.

In summary, there is no cutoff for low contact resistances. Otherwise, the cutoff must be found by constructing the transmission line problem carefully. For practical devices, there appears to be one cutoff frequency²¹. Inspection of Figure 4.10 shows that the cutoff frequency is *never* below $(R_s C)^{-1}$. Finally, Schottky mixing can be easily accounted for once the voltage drops at the contacts are known²². It is to be seen in Chapter 7 whether this model predicts the cutoff frequencies in an adequate manner.

4.6 Conclusions

This chapter concludes our theoretical analysis. We have developed the theory of mixing of a nanotube transistor. When the nanotube corresponds to a single discrete mixer, a dc current appears as a result of an ac bias. If we have Schottky contacts, they will also generate a dc current.

We have also modeled the frequency dependence of this mixing current by treating the nanotube as a lossy transmission line. We have developed the tools to compute the cutoff frequencies, with solutions that are usually non-analytic. In any situation, though, the model predicts a dc voltage to build up in the nanotube so as to keep the current constant. It should be possible to measure a dc voltage build-up with an appropriate probe, such as scanning probe microscopy (Electrical Force Microscopy, for example).

²¹ The plateaus predicted are only pronounced when the device resistance is ~ 100 times more conductive than either contact. That is outside of the typical observed experimental range of resistances.

²² Use $V_{sd} - V(0)$ for the source, and $V(L)$ for the drain. Even then, the amplitude of Schottky mixing, determined by the reverse saturation currents, is not known with certainty.

The mixing experiment will be the subject of Chapter 7. These experiments were performed in the *RC* limit in short nanotubes, and we will discuss how they compare to the theory described in this chapter.

CHAPTER 5

DEVICE PREPARATION AND STANDARD CHARACTERIZATION

5.1 Introduction

Preparation of carbon nanotube devices can be divided into design and fabrication. While design of our devices was generally experiment-specific, our sample fabrication relied on several common steps. One of these, the most important part of the entire fabrication process, was how to obtain the single-walled carbon nanotubes (SWNTs). The two main methods can be described as deposition of the ready-made material or *in situ* growth. The former consists of dispersing carbon nanotubes in solution onto a substrate and then using imaging techniques to locate them and selectively wire them up (Bockrath, Cobden et al. 1997; Tans, Devoret et al. 1997). The latter, on the other hand, consists of patterning catalyst sites on a substrate at specific locations and then growing the material by means of a technique called chemical vapor deposition (CVD)¹. The development of this method for *in situ* growth (Kong, Soh et al. 1998) made it possible to produce more devices per sample in a shorter amount of time, a major step towards applications. We opted for this method in our approach. This was particularly useful in obtaining a large number of devices, thus improving our statistics of the devices' properties.

The two types of design that were used in the experiments of the next two chapters differed mainly in the use of the gate electrode of the nanotube transistor. In the most general case, a degenerately doped silicon substrate with an insulating layer of oxide on top plays the role of one global back-gate electrode that can be used to

¹ This is the same technique described in Chapter 1, except that in this case it is combined with lithographically patterned catalyst.

study any single device fabricated on top of it. This is quite simple to implement from the fabrication point of view, because no lithographic technique is needed to make electrical contact to the gate (a drop of indium solder on a cleaved edge of the sample is enough to accomplish this task). Back-gated devices, on the other hand, are not suitable for high-frequency testing. Source and drain metal leads overlap entirely with the back-gate, generating a very large parasitic capacitance that shorts ac voltages to ground at very low frequencies. The only way of eliminating this capacitance is to use a high-resistivity or an insulating substrate and to fabricate a local gate electrode lithographically which will not overlap with the source and drain leads. We will now describe how both types of samples were fabricated. Later, we will present the results of their standard dc characterization.

5.2 Fabrication of back-gated samples for dc testing

Devices were made as follows (see Figure 5.1 for an overview): using standard optical lithography with the use of a 5:1 Stepper², catalyst pad sites were patterned on ~ 1.5- μm thick photoresist (Shipley 1813) on a degenerately doped four-inch silicon wafer with thermally grown silicon dioxide on the surfaces³. The pattern was then transferred by reactive ion etching with oxygen gas to an intermediate ~ 1.5 μm -thick layer of poly(methyl methacrylate) (PMMA 495 MkW), which was used subsequently as a lift-off mask for the catalyst⁴.

The catalyst consisted of iron in the form of $\text{Fe}(\text{NO}_3)_3 \cdot 9\text{H}_2\text{O}$ mixed with $\text{MoO}_2(\text{acac})_2$ ⁵ and supported by alumina nanoparticles, diluted in methanol. The

² The ratio of 5 gives image reduction of the pattern on the photomask to the size on the sample. The machine was a GCA-6300 5X g-line Stepper.

³ Oxide thickness was 200 nm.

⁴ PMMA was used as a lift-off mask instead of photoresist because methanol, which is used to disperse the catalyst, attacks photoresist but not PMMA.

⁵ Maximum growth output of carbon nanotube is obtained by adding molybdenum to the catalyst (Dai, Rinzler et al. 1996).

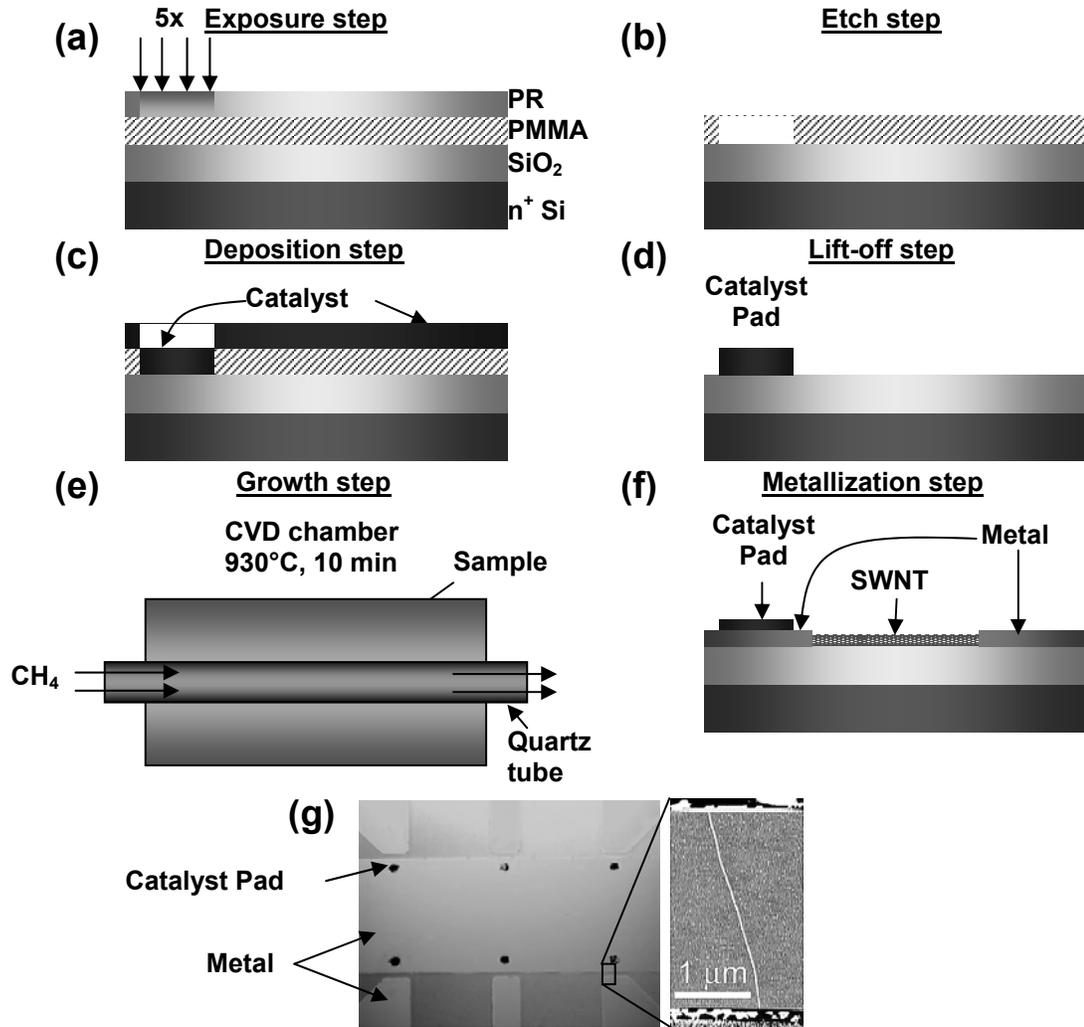


Figure 5.1. Making of carbon nanotube devices by patterned CVD growth. We start with a Si wafer with degenerately doped Si substrate with thermally-grown SiO₂ on its surfaces. **(a)** We deposit a layer of PMMA and a layer of photoresist (PR) on top. Optical lithography (5X Stepper) is used to expose windows in the PR. **(b)** After developing the PR, reactive ion etching (RIE) with O₂ is used to transfer the pattern to the PMMA. It is possible to simultaneously etch away the entire PR. The PR/PMMA interface must be removed. **(c)** Catalyst is deposited over the sample and allowed to dry in air. **(d)** The sample is dipped into 1,2-dichloroethane to selectively remove the PMMA and achieve liftoff of the catalyst, leaving behind patterned catalyst pads. **(e)** The sample is diced so that it can fit into the quartz tube of the CVD chamber (1 inch diameter in our case). The chamber is heated to 930°C in Ar atmosphere, and then CH₄ is allowed to flow for 10 minutes. **(f)** This CVD recipe results in single-walled carbon nanotubes (SWNTs). Metal contacts are deposited by additional lithography and e-gun evaporation. **(g)** Optical micrograph of finished devices and atomic force microscope (AFM) image of a device showing a nanotube. The 5 μm × 5 μm squares are the catalyst pads. The opposite metal ends are 15 μm wide.

solution was carefully stirred and submitted to ultrasonication in order to avert particle aggregation and precipitation before its application to the samples. Droplets covering the whole sample surface were applied, after which the catalyst was allowed to dry in air. Lift-off was done in 1,2-dichloroethane, a solvent that releases the PMMA while allowing the catalyst in direct contact to the wafer surface to remain in place. The chips were then further cleaned with acetone, methanol and isopropanol and blow-dried.

Carbon nanotube growth was then performed in a CVD chamber: the chips were inserted into a quartz-tube furnace which was heated to $\sim 930^{\circ}\text{C}$ in argon atmosphere. At that point, argon was exchanged for methane gas for ~ 10 minutes (growth step). The furnace was then allowed to cool down in argon atmosphere. Previous characterization of such growth (Kong, Soh et al. 1998; Gore 1999) showed a prevalence of single-walled carbon nanotubes⁶. Atomic force microscopy (AFM) shows a diameter distribution between 1 nm and 3 nm, consistent with single-walled nanotubes. Notice that this particular CVD technique does not provide accurate control of nanotube diameter or chirality. Furthermore, the nanotubes tend to grow pointing in random directions and with random lengths⁷. Not all catalyst sites within the same sample produce nanotubes.

Following the growth step, optical lithography was again used to define the electrical contacts to the nanotubes⁸. This was accomplished by electron-gun evaporation of 30-50 nm of the desired metal (usually 5 nm Cr/50 nm Au) followed by lift-off. By evaporating metal contacts next to every catalyst pad, a random fraction of the junctions would have carbon nanotubes bridging the gap between the contacts.

⁶ Individual nanotube walls were characterized by Transmission Electron Microscopy (TEM).

⁷ Recent modifications to the CVD technique have made it possible to grow mm-long nanotubes aligned with gas flow (Huang, Cai et al. 2003).

⁸ Our nanotube lengths are typically a few microns long. By choosing an adequate source-drain separation, it is possible to obtain junctions with one or a small number of nanotubes. Our typical device separations have lengths between 1 and 3 μm .

These could then be identified by performing an electrical measurement. We will return to this step shortly.

Once the devices were finished, an additional annealing step could be done to lower their contact resistances. This step consisted of inserting the devices into the quartz-tube furnace with argon flow at 600°C for 45 minutes. The contact resistance between nanotubes and metal leads was typically reduced by one order of magnitude when chrome/gold contacts were used.

5.3 Fabrication of top-gated samples for ac testing

Top-gated samples were also made by optical lithography, therefore several of the fabrication steps used in making the dc samples were repeated. For example, the nanotubes were grown by CVD following the same steps prior to evaporation of the metal contacts⁹. Instead of repeating the description of these steps, we will detail the ones specific to ac top-gated samples.

The substrate used was made of high-resistivity silicon (in range 12-39 kΩ-cm) with 1 μm-thick thermal SiO₂ grown on its surfaces. The purpose of these materials was to reduce the capacitances of the leads with the substrate, as mentioned in Section 5.1. Then, we adopted a design for the leads known as a coplanar waveguide (CPW, Pozar 1998), compatible with our high-frequency probes and made of 5 nm Cr/50 nm Au/10 nm Au-Pd alloy. It consisted of three equally spaced conductive strips used in the ground-signal-ground configuration (GSG), and it was designed as follows: signal contact pad was a 50 μm square; gap between strips was 50 μm; extension of ground pads was designed to accommodate both 100 μm and 150 μm-pitch GSG probes;

⁹ The high temperatures of CVD growth forbid the use of most metals, with the exception of those with high melting temperatures such as Mo or W.

distance from contact pads to catalyst pad was $\sim 250 \mu\text{m}$ ¹⁰; and the symmetry of the CPW was exploited such that occasional long nanotubes bridging between ground (drain) lines could be gated on either side of the signal (source) line (see Figure 5.2).

In the next step, source and drain contacts to the nanotubes were made of 50 nm Pd¹¹ and contacted electrically to the CPW from the top. Then, a local gate oxide was made by liftoff of 10 nm evaporated¹² SiO₂, and a 50 nm Al gate electrode was evaporated on top, finishing the top gate. Aluminum was used as the top gate electrode because of two reasons: it was found to make extremely poor electrical contact to nanotubes, a desirable property in the event of physical leakage of Al through the gate oxide¹³; and it is one of the most conductive metals, ideal for use in CPWs. The top gate made electrical contact to the CPW from the top¹⁴.

The finished devices had source-drain gaps of $\sim 3 \mu\text{m}$ with $\sim 2 \mu\text{m}$ under the gate electrode, and the gate electrode slightly overlapped with the center source electrode by $\sim 100 \text{nm}$ ¹⁵.

Because of the high impedances of nanotube devices, it was hard to use these CPWs for direct high-frequency measurements (as described in the introduction of Chapter 4). In order to measure our devices as frequency mixers instead, it was necessary to cut the ground line of the CPW to separate it from the drain (detection)

¹⁰ Distance from probe/ contact pad to device was kept below $\lambda/20$ of the wavelength at 50 GHz to avoid length-dependent modulation of the ac voltage at that frequency. That corresponds to a limit of $\sim 300 \mu\text{m}$ in air.

¹¹ Javey (Javey, Guo et al. 2003) showed that it is possible to obtain low-resistance contacts to nanotube with Pd.

¹² Evaporation, as opposed to plasma-enhanced chemical vapor deposition (PECVD), was shown to leave device conduction nearly intact (Ganguly, Zhang et al. 2005).

¹³ Aluminum has also been reported as an n-type contact to nanotubes (Javey, Wang et al. 2003).

¹⁴ It is well-known in metallurgy that gold and aluminum make poor electrical contact to each other. Au/Pd alloy was used as the top layer of the CPW because it is a common adhesion layer for the two materials.

¹⁵ This was a property of the devices measured in Chapter 7. Ideally, obtaining perfect alignment in the lithography would result in no overlap.

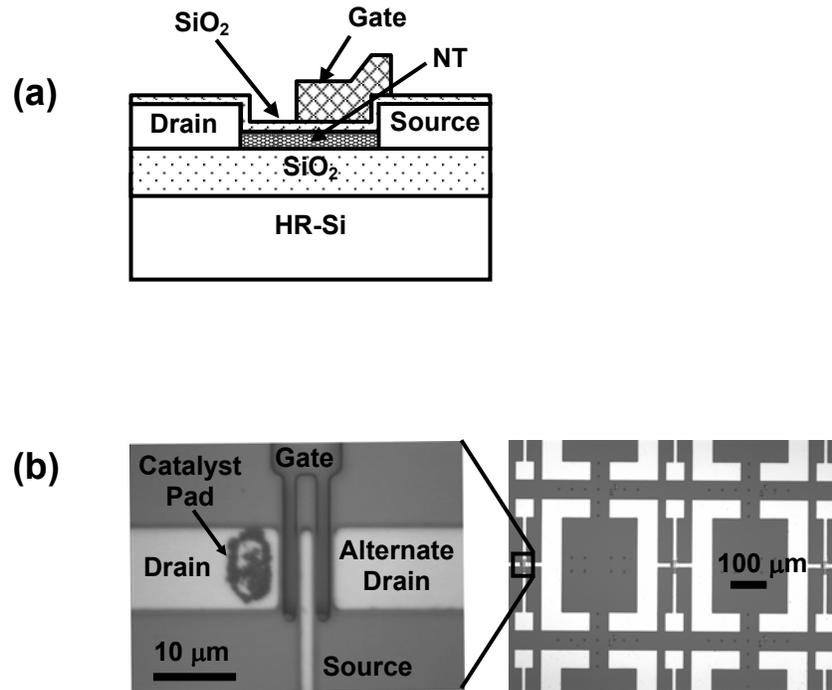


Figure 5.2. Design of top-gated devices. **(a)** Schematic cross-section of device, layers not to scale. The oxide thicknesses are 10 nm for the top gate and 1 μm for the back gate. Top gate is portrayed with a slight overlap with the source contact. No overlap results under ideal alignment circumstances. Catalyst pad not shown. **(b)** Optical micrographs of top-gated devices. Coplanar waveguide (CPW) geometry was chosen for high-frequency testing. An alternate drain electrode is available in case a nanotube grows long enough.

line. This was done for the experiment of Chapter 7. Since the electrodes were found to peel easily when scratched, a dc probe was used to physically split the ground line in two, as shown schematically in Figure 5.2. After accomplishing the split, the source could be probed with a GSG probe (see details of probing in Chapter 7), while the gate and drain could be probed with dc probes.

5.4 Standard characterization

Regardless of the type of sample prepared, the next step is to find which junctions were successful at producing a nanotube bridging the gap between the source and drain electrodes, and subsequently to characterize their basic electrical properties, such as which devices are metallic and which are semiconducting. The standard method of characterization for all the samples is the application of a small bias V_{sd} to the source, typically 10 mV in our experiments, and to measure the dc current at the drain while sweeping the gate voltage V_g . Generally, metallic nanotubes display a constant electrical current with respect to gate voltage, whereas the current changes with gate voltage for semiconducting nanotubes. Three such measurements are displayed in Figure 5.3, measured for back-gated devices. Notice that the semiconducting nanotubes are always found to be normally-on and p-type when fabricated in this manner (see definitions in Chapter 3). Also notice that Figure 5.3 (c) has a small band gap but the device does not shut off completely. This is believed to be a metallic nanotube with a deformation or defect which opens a band gap (Zhou, Kong et al. 2000). In fact, metallic nanotubes with no band gaps are rarely seen.

Despite the variable (typically 10-30%) yields of successful nanotube bridging per total number of junctions per sample fabricated, this preparation method can be regarded as mass-production of nanotube devices. We can then gather some statistics

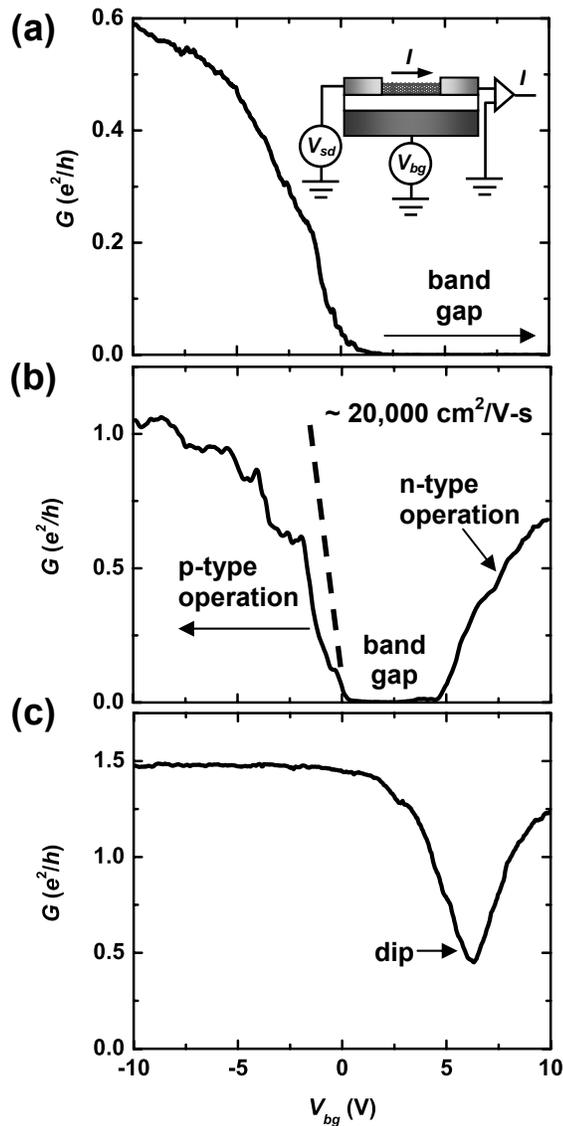


Figure 5.3. Conductance versus back-gate voltage measurements. Source-drain bias of 10 mV. **(a)** Semiconducting nanotube device exhibiting clean p-type behavior. The device turns off (band gap region) for positive gate voltage. Notice that it conducts even at zero gate voltage. **(b)** Ambipolar device. Operation in the p-type, band gap and n-type regions is illustrated. Notice that the device conducts at zero gate voltage and the n-type region is less conductive than the p-type region. The dashed line corresponds to the slope used to extract the value of hole mobility, $20000 \text{ cm}^2/\text{V-s}$ in this case. **(c)** Small-bandgap device. There is a dip in the conductance and the conductance at positive gate voltage is slightly lower than at negative gate voltage.

on a relatively large number of devices. The quantities that we are mostly interested in are the on-state conductance and the field-effect mobility of semiconducting nanotubes. While we measure the on-state conductance at the most negative value of our V_g range, the mobility can be experimentally determined from (see Chapter 3):

$$\mu_{FET} = -\frac{L}{C_g'} \frac{\partial G}{\partial V_g}, \quad (5.1)$$

where L is the length of the device, C_g' is the total gate capacitance per unit length and G is the low-bias conductance. The length is determined by the design, the derivative is determined by the slope of the conductance sweep, and the capacitance of a back-gated device with 200 nm of gate oxide was estimated in Chapter 2 to be approximately 3.7×10^{-17} F/ μm for a 2 nm-diameter nanotube. This estimate neglects the effect of the overlapping contacts, and instead we use here the value 2×10^{-17} F/ μm extracted from Coulomb-blockade measurements (Bockrath, Cobden et al. 1997; Tans, Devoret et al. 1997; Cobden, Bockrath et al. 1998).

The variation of the on-state conductance and the field-effect mobility of our back-gated devices are shown in the histograms of Figure 5.4. We find that the best conductances are within a factor of 4 from the quantum limit of $G_Q \sim 155 \mu\text{S}$, an indication that we have indeed devices of good contact quality. The typical mobilities, on the other hand, are found in the range 1000 to 4000 $\text{cm}^2/\text{V}\text{-s}$. This is consistent with the expectations of hole mobility in all-carbon-based devices, since it is known that the mobility in graphite is also in the thousands ($\sim 8000 \text{ cm}^2/\text{V}\text{-s}$). In a few instances, as seen in the histogram, the mobilities can be even higher. Recent

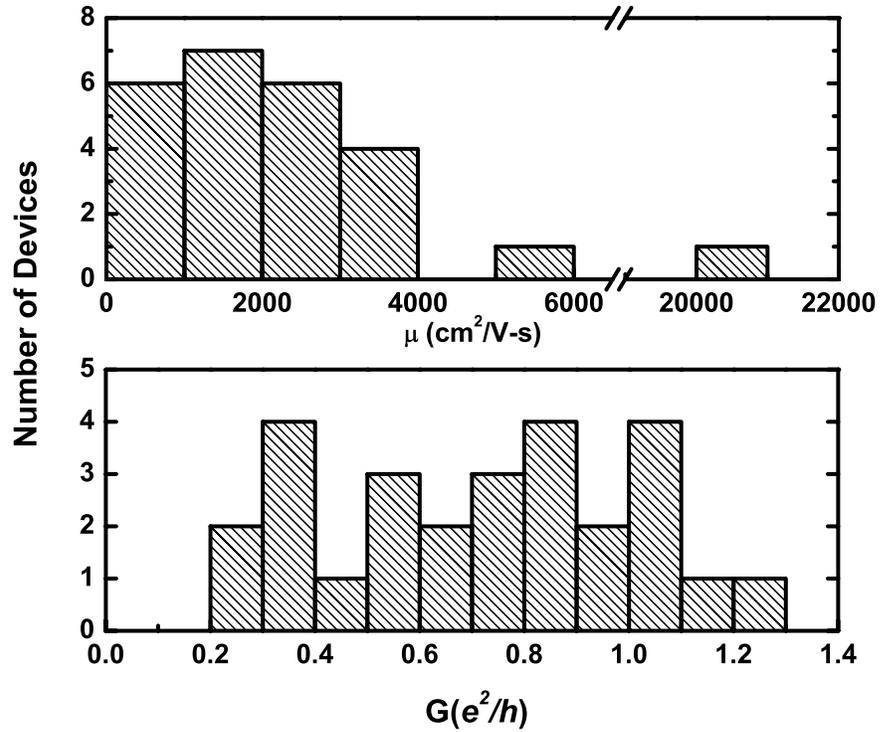


Figure 5.4. Histogram of hole mobilities and maximum on-state conductances determined from measurements of individual SWNTs in vacuum. The data point corresponding to the mobility of $20000 \text{ cm}^2/\text{V}\cdot\text{s}$ corresponds to the device of Figure 5.3 (b).

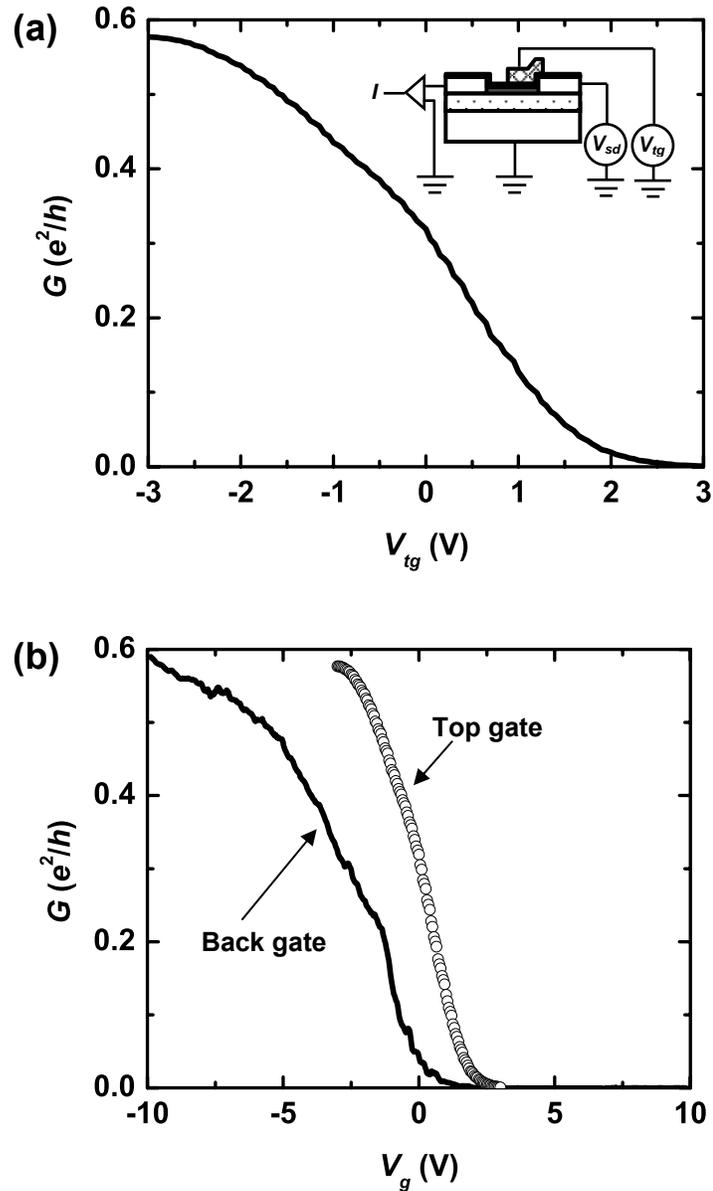


Figure 5.5. Conductance of a top-gated device. **(a)** Conductance of a semiconducting device with a top gate. **(b)** Comparison between the conductances of two *different* devices with similar on-state conductances ($\sim 0.6 e^2/h$). The top-gated device is the same of part (a), while the back-gated device is the same of Figure 5.3 (a). Notice that the range of gate voltage from on- to off-state is smaller for the top-gated device due to the improved gate capacitance.

developments indicate that the devices with anomalously high mobilities have defects which control their values (Zhou, Park et al. 2005).

Finally, the electrical characteristics of a top-gated semiconducting device of the kind that will be used in Chapter 7 are shown in Figure 5.5. As pointed out in Chapter 2, the capacitance of the top gate that we fabricated is roughly only twice the capacitance of our back-gated devices. This is evident from the figure, since the slope is slightly steeper. The result is that a smaller overvoltage is required in order to switch the device on or off.

5.5 Conclusions

We fabricated single-walled carbon nanotube devices by means of CVD growth and optical lithography. This approach made it possible to efficiently study large amounts of nanotube devices. Typical on-state conductances were found to be within order-of-magnitude from the quantum conductance limit, an indication of low-resistance contacts. The mobilities were found to be comparable to that of graphite.

Back-gated devices were used in the electrolyte-gating experiment and will be the subject of the next chapter. The top-gated samples on resistive substrate were used in high-frequency experiments that will be described in Chapter 7.

CHAPTER 6

ELECTROLYTE-GATING OF CARBON NANOTUBE TRANSISTORS

6.1 Introduction

The most immediate application of a semiconducting carbon nanotube is as the active channel of a field-effect transistor (FET). A technologically relevant FET must have a high on/off current ratio¹, low on-state impedance², high field-effect mobility³, low subthreshold swing⁴, and high transconductance⁵. Most of these properties have been defined in Chapter 3.

The main experimental parameters that can be adjusted are the contact resistances and the gate properties. Considerable progress towards low-resistance contacts has already been made through improvements to fabrication of the metal-nanotube junctions. Low resistances have been observed in short devices⁶, nearing half of the ballistic conduction limit of $4e^2/h \sim 155 \mu\text{S}$ (Javey, Guo et al. 2003; Yaish, Park et al. 2004). The gate properties, on the other hand, are represented by the transconductance and the subthreshold swing and depend on optimization of the gate capacitor. Several groups have recently realized devices in a top- or bottom-gate geometry using high-dielectric-constant dielectrics (Javey, Kim et al. 2002; Appenzeller, Lin et al. 2004; Kim, Brintlinger et al. 2004), showing next-to-ideal

¹ Two different logic states must be significantly distinguishable, therefore requiring a large on/off current ratio. On/off current ratios of order 10^6 have become routine (Martel, Derycke et al. 2001; Wind, Appenzeller et al. 2002; Javey, Guo et al. 2003; Javey, Wang et al. 2003).

² Enough current must flow in order to power a load. In order to accomplish this with a minimal supply of power, the impedance of the nanotube must be minimized. Ideally this should be 50Ω .

³ As seen in Chapters 3 and 4, a high mobility implies a fast switch. Mobilities should be similar to that of bulk graphite ($\sim 10^4 \text{ cm}^2/\text{V}\cdot\text{s}$).

⁴ As discussed in Chapter 3, the subthreshold swing is one measure of how fast the switch is near the threshold. The thermal limit is $\sim 60 \text{ mV/decade}$ at room temperature.

⁵ As seen in Chapter 3, the transconductance is a measure of the device's sensitivity to the environment.

⁶ Near the ballistic limit where the length of the nanotube is much shorter than the mean-free-path for electron-phonon scattering.

characteristics. Prior to these results, we used of an electrolyte gate to create a high transconductance carbon nanotube transistor (Rosenblatt, Yaish et al. 2002). Our results were important not only for transistor applications but also for biological and chemical sensing applications. These results are the scope of this chapter. We will discuss FET characterization of electrolyte-gated carbon nanotube transistors using the quantities and definitions of Chapters 2 and 3. We will show that the electrolyte gate is in the quantum capacitance limit, a realization of the ideal gate geometry described in Chapter 2.

6.2 Devices and setup

Nanotubes were grown as described in Chapter 5 on degenerately doped silicon wafers with 200 nm of thermally grown silicon dioxide. Following the growth step, optical lithography was used to define the electrical contacts to the nanotubes, accomplished by electron-gun evaporation of 5 nm Cr/ 50 nm Au followed by lift-off. The finished devices, with source-to-drain separations of 1 to 3 μm , were once more inserted into the quartz-tube furnace for an annealing step, consisting of argon flow at 600°C for 45 minutes. This step was shown to significantly reduce contact resistance between the nanotubes and the electrodes, typically by an order of magnitude.

The experimental setup for doing electrolyte gating follows the approach pioneered by Krüger et al. to study multiwalled carbon nanotubes (Kruger, Buitelaar et al. 2001). As shown in Figure 6.1, a micropipette was used to place a small ($\sim 10\text{-}20$ μm diameter) water droplet onto a nanotube device. A voltage V_{wg} applied to a silver wire in the pipette was used to tune the electrochemical potential in the electrolyte relative to the device, which was grounded at the drain end. Typically, for $-0.9\text{ V} <$

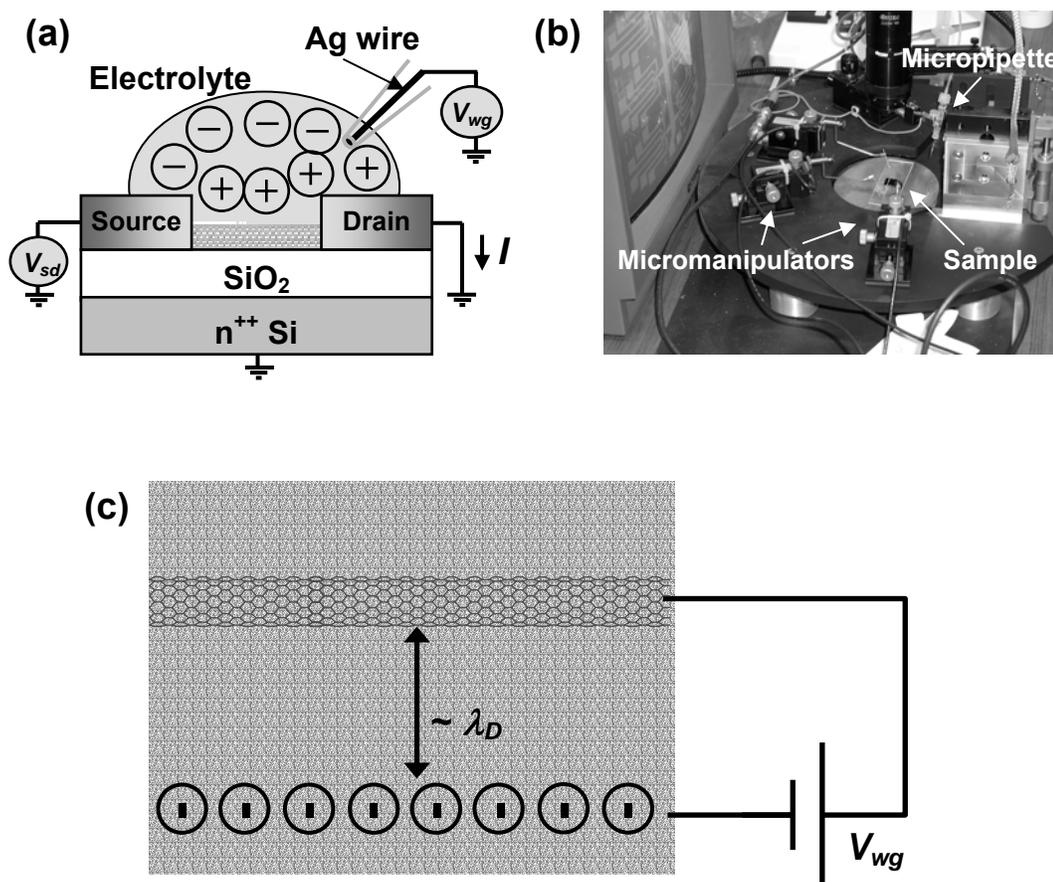


Figure 6.1. Electrolyte-gating experimental setup. **(a)** Schematic. Gate voltage V_{wg} is applied to the silver wire running inside a micropipette, setting the electrical potential in the microdroplet of electrolyte. Nanotube is grown on a degenerately doped silicon wafer with ~ 200 nm thermal oxide insulating layer. Source-drain voltage V_{sd} is applied to the nanotube through patterned gold electrodes, and the current is detected at the drain. **(b)** Photograph of experimental setup. Micromanipulators are used to control electrical probes and micropipette. **(c)** Concept of electrolyte-gating. Gated ions in solution are assumed to make a wrap-around gate capacitor with the nanotube at a distance of order of the Debye length (see Chapter 2).

$V_{wg} < 0.9 \text{ V}$ ⁷, the leakage current between the water and the gold electrodes/nanotubes was negligible (less than 1 nA). Because of this, the liquid-gate could be regarded as well-insulated. Outside this range, the electrolyte in the water reacted with the gold electrodes, degrading the physical properties of the device.

6.3 Transistor characteristics

The low-bias conductance G versus V_{wg} for a source-drain bias of 10 mV is shown in Figure 6.2 for three nanotubes of increasing diameters. The electrolyte is 10 mM NaCl⁸. P-type conduction can be seen with all three devices for negative V_{wg} . For positive V_{wg} , n-type conduction is also possible. Both Figures 6.2 (b) and (c) display *ambipolar* behavior (as defined in Chapter 1). This is strongest for Figure 6.2 (c), because the conduction is never zero.

The inset of Figure 6.2 (a) shows the low-bias conductance of the corresponding device probed dry in vacuum, plotted against the back-gate voltage V_{bg} (this voltage is applied directly to the degenerately doped substrate). Although the conductance levels are similar, more voltage (overvoltage⁹) must be applied to the back-gate in order to obtain the same amount of current.

The inset of Figure 6.2 (b) shows the conductance of the corresponding device in a logarithmic scale. The subthreshold swing, defined in Chapter 3 as $S = [d(\log I_{sd})/dV_g]^{-1}$, is $\sim 80 \text{ mV/decade}$ (similar values were obtained for other

⁷ Referenced to either the source or drain electrode. Assume for now that we are in the low-bias regime, so both source and drain can be regarded as ground.

⁸ Other salts were used, such as MgSO₄ and NaNO₃, with no advantage observed regarding threshold value, electrode degradation potential or gate strength. Salts with higher chemical valence have shorter screening length and should have a stronger gate effect if the capacitance is of entirely electrostatic nature.

⁹ As defined in Chapter 3, the gate overvoltage measures the gate voltage distance to the gate threshold, $V_o = |V_{g0} - V_g|$, once the device is conducting.

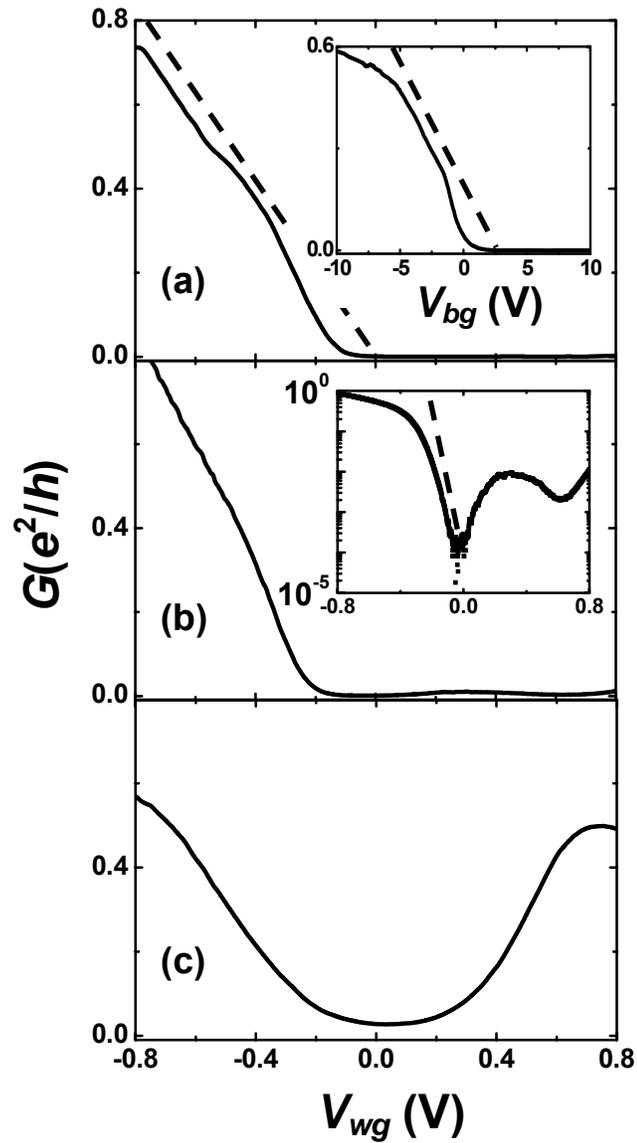


Figure 6.2. Conductance G versus electrolyte gate voltage V_{wg} for three nanotubes. The lengths and diameters (as measured by atomic force microscopy – AFM) are given by: **(a)** $L = 1 \mu\text{m}$, $d = 1.1 \text{ nm}$, **(b)** $L = 1.4 \mu\text{m}$, $d = 3 \text{ nm}$, and **(c)** $L = 2.2 \mu\text{m}$, $d = 4.3 \text{ nm}$ wide. Inset to **(a)**: G versus the back gate voltage V_{bg} for that device measured in vacuum; the slope of linear regime is given by dashed line. Inset to **(b)**: Logarithmic scale plot showing the exponential dependence of G on V_{wg} for that device.

electrolyte-gated devices). This is very close to the theoretical upper limit of $S = 60$ mV/decade at room temperature¹⁰.

We now map the current in the device simultaneously as a function of source-drain and electrolyte-gate biases. We perform this experiment in all of the allowed phase space of these parameters, delimited by the boundaries determined by the reaction potentials of the electrolyte with the metallic electrodes¹¹. As mentioned earlier, this boundary is typically set by $-0.9 \text{ V} < V_{wg} < 0.9 \text{ V}$ at low source-drain bias. At high source-drain bias, we must have both $|V_{wg} - V_{Source}|$ and $|V_{wg} - V_{Drain}| < 0.9 \text{ V}$. If we set $V_{Drain} = 0$, then $|V_{wg} - V_{Source}|$ and $|V_{wg}| < 0.9 \text{ V}$.

The result is seen in the color plot of Figure 6.3, which corresponds to the same device as Figure 6.2 (b) probed with 10 mM NaCl. The color scale represents the current in the device in a logarithmic scale. The blue trapezoid of low conductance in the center corresponds to the band gap region. The red regions to the left of the trapezoid correspond to p-type conductance, while those to the right correspond to n-type conductance.

The trapezoid is delimited by two vertical lines and two slanted lines. The vertical lines correspond to the gate thresholds for p- and n-type conduction (negative and positive V_{wg} 's, respectively). The thresholds can be determined from these lines as $V_{g0} = V_g$ (-0.1 V and +0.35 V, respectively, from the figure). The slanted lines have a slope of $dV_{sd}/dV_{wg} \approx 1$.

¹⁰ Recent improvements using solid-state gate engineering showed that it is possible to circumvent this limit by controlling band-to-band tunneling in short devices. A value of 40 mV/decade has been measured in the n-region (Appenzeller, Lin et al. 2004).

¹¹ As mentioned earlier, the electrolyte in the water droplet can chemically react with the metallic contacts because they are in physical contact in our setup. This causes electrical degradation in our devices. This range was determined experimentally.

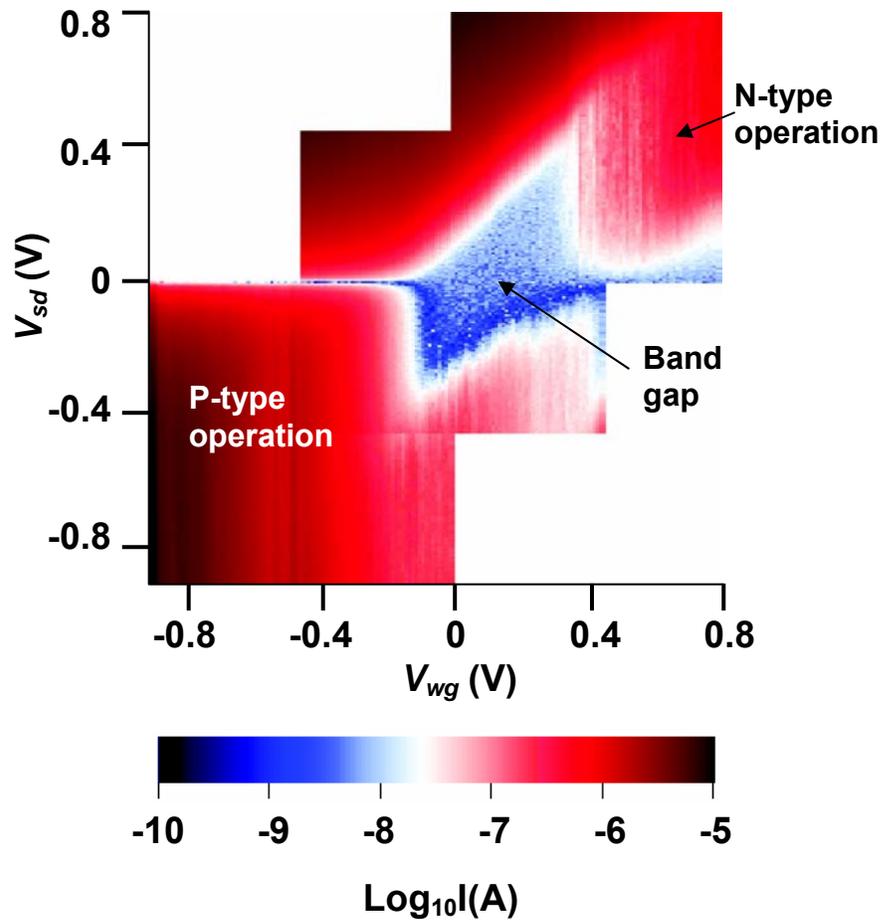


Figure 6.3. Colorscale plot of current on a logarithmic scale versus V_{wg} and V_{sd} for the device of Figure 6.2 (b). The bandgap region is given by the blue trapezoid at the center. The threshold gate voltages for p- and n-type operation are extracted from the vertical edges of the trapezoid.

6.4 Quantum gate capacitance limit

As discussed in Chapter 2, the total gate capacitance is $C_{total} = (C_E^{-1} + C_Q^{-1})^{-1}$, where C_E is the electrostatic capacitance and C_Q is the quantum capacitance. With enough overvoltage, the quantum contribution should be a constant (per unit length): $C_Q' = 8e^2/hv_0 \sim 3.86 \times 10^{-10}$ F/m. Typical electrostatic capacitances in a coaxial cable configuration with such dimensions and SiO₂ dielectric are much smaller, and therefore dominate the total capacitance. But due to the high dielectric constant of water, $\kappa \sim 80$, it is possible to have the quantum capacitance be the smaller of the two, in which case the total capacitance is limited by the quantum limit.

We will use the concept of field-effect mobility, as defined in Chapter 3 for a p-type FET, to quantify the capacitance:

$$\begin{aligned} \mu_{FET} &= -\frac{L}{C_g'} \frac{\partial G}{\partial V_g} \\ \Rightarrow -\frac{\partial G}{\partial V_g} &= \frac{\mu_{FET}}{L} C_g' \end{aligned} \quad (6.1)$$

where L is the length of the device, C_g' is the total gate capacitance per unit length and G is the low-bias conductance. The slope of G versus V_g is a measure of the gate strength. Back to Figure 6.2 (a), the slope is $\sim 0.08 e^2/h/V$ ($3 \mu\text{S/V}$) with back-gate in vacuum and $\sim 1 e^2/h/V$ ($38.8 \mu\text{S/V}$) with 10 mM NaCl electrolyte gate. These are a factor of ~ 10 apart. The electrostatic capacitance of the back-gate in this wire-on-plane geometry (see Chapter 2) is $\sim 3.4 \times 10^{-17}$ F/ μm , about 10 times smaller than the quantum capacitance (Chapter 2) of $C_Q' \sim 3.86 \times 10^{-16}$ F/ μm . On the other hand, the electrostatic capacitance of the electrolyte-gate using a cylindrical capacitor model¹²

¹² Also seen in Chapter 2, a 10 mM NaCl solution has a Debye screening length of $\lambda_D \sim 3$ nm, which in this model we use as the distance between the nanotube's surface and the outer conductor's shell.

(see Chapter 2) is $\sim 2.4 \times 10^{-15}$ F/ μm , approximately 10 times larger than C_Q' and 70 times larger than the back-gate's electrostatic capacitance. If we assume that the mobility has not changed upon application of the droplet, then according to Equation 6.1 the capacitances must have changed. This means that the total capacitance in the electrolyte-gate case must be limited by the quantum capacitance. Note that the dielectric constant of water is not 80 at short distances, so the electrostatic capacitance of the electrolyte-gate must be somewhat lower, perhaps with similar strength as the quantum capacitance (Teschke, Ceotto et al. 2000). In spite of that, when the electrolyte concentration was increased to ~ 1 M, the slope did not change. All this points to is that indeed we find ourselves at the quantum capacitance limit of the gate.

In order to characterize the gate properties further, we measure the devices' properties in the nonlinear regime, as illustrated by Figure 6.4. This corresponds to the same device as Figure 6.2 (b) and the same dataset as Figure 6.3. Figure 6.4 (a) shows the current versus source-drain bias at different electrolyte-gate voltages, in the p-region (negative V_{wg}). Current saturation at large negative bias in the electrolyte-gate experiment is due to pinch-off, when V_{sd} becomes of order the overvoltage $|V_{wg} - V_{wg0}|$. We notice that although the current is saturating, the current gap between consecutive gate voltage steps increases with gate overvoltage. As defined in Chapter 3, the transconductance in the saturation region, $g_m = dI/dV_{wg}$, measured at $V_{sd} = -0.8$ V, grows approximately linearly with $|V_{wg} - V_{wg0}|$, as shown in Figure 6.4 (b), and reaches a value of 20 $\mu\text{A/V}$ ($[\mu\text{S}]$) at $|V_{wg} - V_{wg0}| \sim 0.7$ V. Measurements on other samples give comparable results. On the other hand, the theoretical prediction of Chapter 3 gives $g_m = -(\partial G/\partial V_{wg})|V_{wg} - V_{wg0}| = (3 \mu\text{S/V}) \cdot (0.7 \text{ V}) \sim 27 \mu\text{S}$, in good agreement with the experimental finding.

Normalizing the transconductance to the device width of ~ 3 nm gives $g_m/d \sim 7 \mu\text{S/nm}$. This is an order of magnitude greater than the transconductance per unit width

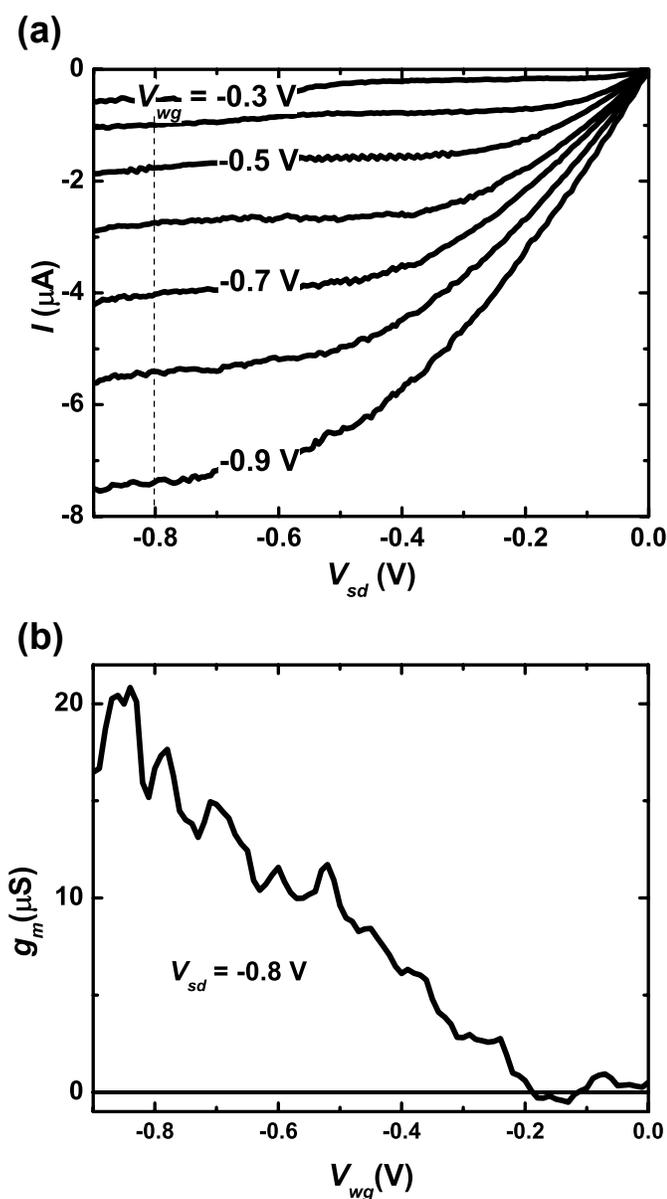


Figure 6.4. Current versus voltage characteristics of electrolyte-gated device. (a) I - V_{sd} characteristics of the device shown in Figure 6.2 (b) at different electrolyte gate voltages ranging from -0.9 V to -0.3 V in 0.1 V steps (bottom to top), extracted from the color plot of Figure 6.3. (b) Transconductance $g_m = dI/dV_{wg}$ taken at $V_{sd} = -0.8\text{ V}$ (dashed line in (a)).

for current-generation MOSFETS¹³. Recent reports have shown that such values of transconductance can also be approached by use of solid-state gates with high- κ dielectrics (Javey, Kim et al. 2002).

The quantum capacitance limit and the high transconductances highlight charge sensing as a possible application. A nanotube is extremely sensitive to the immediate charge environment (concentration of surrounding ions), with large current changes brought upon by small changes in gate voltage (which can also be induced by nearby charged objects). For successful (non-specific) detection of individual charged species (such as DNA, whose width is ~ 2 nm, comparable to the nanotube), the gate voltage in solution could be adjusted to the point of maximum sensitivity, so that a charge passing in the vicinity of the nanotube would induce a distinct current change.

A last way of characterizing the gate is in its efficiency to modulate the band energies. We first look at the inset of Figure 6.2 (b). As discussed in Chapter 3, in the thermal activation regime $I \sim \exp(-E_b/kT)$, where E_b is the energy from the Fermi level to the nearest of the conduction and valence bands. This barrier height changes linearly with respect to the gate: $\delta E_b = e\alpha\delta V_g$, where α is a numerical constant that measures the effectiveness with which the gate modulates the band energies. Ideally, 1 V in the gate would translate into a 1 V change in the Fermi level of the nanotube. We obtain the value of α from the value of the subthreshold swing S from the definition of Chapter 3, $S = (kT/\alpha e) \cdot \ln 10$. A swing of 80 mV/decade implies $\alpha \sim 0.75$.

The constant α can then be used to infer the band gap of the nanotube of Figure 6.3. From the measured width of the gap $\Delta V_{wg} \sim 0.45$ V, we obtain $E_g = e\alpha\Delta V_{wg} \sim (0.75) \cdot (0.45 \text{ eV}) = 0.33 \text{ eV}$. This is in reasonable agreement with the expected value for a 3-nm tube obtained from the relation¹⁴ $E_g = 0.8 \text{ eV}/d [\text{nm}] \sim 0.27$

¹³ This comparison assumes that it is possible to stack identical, non-interacting nanotubes in parallel in order to constitute a bulk material.

¹⁴ Note that the size of the gap between n- and p-behavior is predicted to decrease with increasing nanotube diameter, as can be observed with the three devices of Figure 6.2.

eV (Wildoer, Venema et al. 1998). What we conclude is that additionally to the gate being in the quantum capacitance limit, the gate coupling is nearly ideal¹⁵.

6.5 Conclusions

Single-walled carbon nanotubes are a promising material for next-generation electronics. The electrolyte-gate experiment allows us to peek into the ultimate limits of gate operation for nanotube FETs. The experiment revealed the existence of the quantum gate capacitance limit and a near-ideal subthreshold swing of 80 mV/decade. Solid-state gates with high- κ dielectrics should consequently be designed to operate at these limits, with immediate applications in fast-switching transistors.

The ultimate limit would be a ballistic (shorter than mean-free-path for phonon scattering) nanotube transistor with a gate capacitance given by C_Q' and transconductance $g_m = 4e^2/h \sim 155 \mu\text{S}$. The devices reported here are within a factor 5-10 of this limit and are quite long ($\sim 1 \mu\text{m}$) – a reduction to $\sim 200 \text{ nm}$ should approach the ballistic limit if contacts can be made ideal.

The experiments also point to an important application in solution. Due to the record-high capacitances and transconductances, it should be possible to realize single-molecule detection.

¹⁵ In addition to the subthreshold, the fact that $dV_{sd}/dV_{wg} \approx 1$ for the slanted lines in the band gap diamond of Figure 6.3 also means that the strength of the electrolyte surrounding the nanotube is identical to the strength of the source and drain electrodes at the ends.

CHAPTER 7

MIXING AT 50 GIGAHERTZ WITH A SINGLE-WALLED CARBON NANOTUBE TRANSISTOR

7.1 Introduction

Since carbon nanotubes have high mobilities, high transconductances and long mean-free-paths¹ (Javey, Kim et al. 2002; Rosenblatt, Yaish et al. 2002; Wind, Appenzeller et al. 2002; Javey, Guo et al. 2003; Kim, Brintlinger et al. 2004; Yaish, Park et al. 2004), they should work as high-frequency transistors. A short single-walled nanotube operating in the ballistic regime and at the quantum capacitance limit is theoretically expected to provide gain at frequencies above a terahertz (Burke 2004).

A recent interest in these high-frequency applications by several groups has led to reports of transmission through nanotube devices and rectification applications. In the first class of experiments, the reflection/transmission properties (Pozar 1998) of carbon nanotube transistors in the microwave regime were measured by standard S-parameter techniques (Huo, Zhang et al. 2004). Unfortunately, such techniques are limited by the extremely high overall impedances of the nanotube devices when compared to the standard 50 Ω characteristic impedance of the test equipment. The S-matrix elements measured in this manner are difficult to distinguish from an open circuit². Nevertheless, some preliminary data have been taken from such experiments: measurements of the ac conductance of metallic nanotubes (Yu and Burke 2005) have shown it to be similar to the dc conductance up to 10 GHz, while semiconducting

¹ See Chapters 2, 3 and 4.

² An open circuit reflects 100% of the input power. As a consequence, no power is delivered to the load. From the voltage viewpoint, this means that the input voltage drops entirely across a high-impedance load. Typical ac voltage sources are designed to match a 50 Ω load, for which the power delivered is maximized and the applied voltage equals half of the source voltage.

nanotubes have been shown to retain the gate sensitivity when used as a component in a 2.6 GHz-resonant circuit (Li, Yu et al. 2004).

Rectification or mixing is another high-frequency technique, particularly useful when dealing with transistors, diodes and other nonlinear devices. This technique was applied to nanostructures to study charge sensitivity of a single-electron transistor up to 300 MHz (Knobel, Yung et al. 2002); current gain in semiconducting nanotubes up to 580 MHz (Appenzeller and Frank 2004); and detection of mechanical vibrations of suspended semiconducting nanotubes up to 500 MHz (Sazonova, Yaish et al. 2004).

In this chapter, experimental results of mixing with nanotubes will be shown at frequencies as high as 50 GHz (Rosenblatt, Lin et al. 2005). We find there is a cutoff frequency that lies in the 1-10 GHz range. The reasons for this cutoff will be discussed using the theoretical model introduced in Chapter 4. Regardless of the mechanism responsible for attenuation, however, this experiment shows that nanotube transistors can be operated as mixers at frequencies as high as 50 GHz.

7.2 The mixing technique

The guiding principle of mixing is that nonlinearities can transfer ac power from the main frequency components of the excitation to other specific frequencies corresponding to various linear combinations of the original frequencies and their harmonics. Detection of the output ac power at one of the low-frequency components should then carry information about both the high-frequency and nonlinear properties of the device. Experimentally, low-frequency detection can be done with the use of a lock-in amplifier. In the limit where the ac signal is completely rectified, a dc amplifier can be used instead. Rectification is a result of the more general phenomenon of frequency mixing (see Chapter 4), and will be referred to as such in the discussion that follows.

The analytical results which we will use in order to understand mixing have been laid out in Chapter 4. The small-signal analysis of a field-effect transistor (Pozar 1998) from Equations 4.3 and 4.8 gives us that the dc mixing current is:

$$\begin{aligned} I_{sd,mix}^{dc} &= -\frac{1}{4} \frac{\partial G(\omega)}{\partial V_g} (V_s^{ac})^2 \\ &= -\frac{1}{2} \frac{\partial G(\omega)}{\partial V_g} (V_s^{ac,rms})^2 \end{aligned} \quad (7.1)$$

where $G(\omega)$ is the device's conductance at frequency ω , V_g is the gate voltage and V_s^{ac} is the ac signal. The last line displays the conversion factor to rms units³. This effect – dc detection of an ac property – is the basis of our experiment.

7.3 Mixing experimental setup

The samples used for the high-frequency experiment were top-gated devices made on a high-resistivity substrate, as described in Chapter 5. The experimental setup for the high-frequency measurements is depicted in Figure 7.1. The experiment was performed at room temperature in a full 4-inch wafer, 6-arm probe station⁴ with interface for two custom-made microwave probes⁵. The electrical probe used for the source was a ground-signal-ground probe (GSG⁶), and the ac source spanned from 10 MHz to 50 GHz⁷. All the components used in the ac signal path were rated for operation up to 50 GHz⁸. Measurements were performed in vacuum to minimize

³ This expression was shown in Chapter 4 to account for both p- and n-type behavior. This means that semiconducting nanotubes which display both polarities (such as *ambipolar* or *small-bandgap* devices), can be analyzed by means of this same equation in any gate regime.

⁴ Desert Cryogenics.

⁵ GGB Industries Picoprobe Model 50A.

⁶ As detailed in Chapter 5, the signal is transmitted through the inner pin and the outer ones are grounded.

⁷ HP 83650 synthesized swept-signal generator.

⁸ The suitable coaxial connectors for 50 GHz operation are air-filled and have a 2.4 mm diameter for the inner side of the outer conductor. These are subsequently named 2.4 mm connectors.

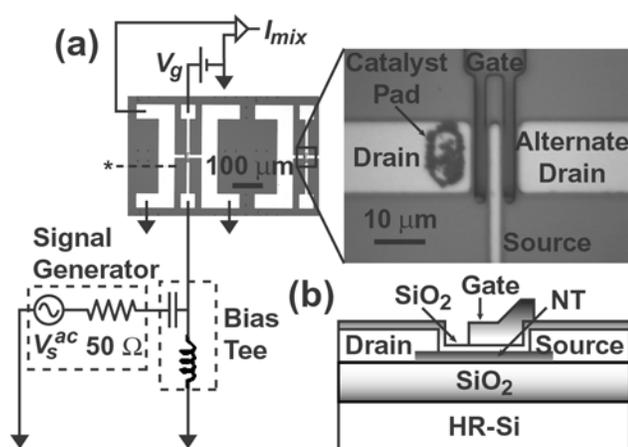


Figure 7.1. Experimental setup for dc mixing with carbon nanotube FETs. **(a)** Optical micrograph of nanotube device along with circuit schematic. The back gate voltage applied to the substrate is not shown. A high-frequency probe delivers the ac signal V_s^{ac} to the source electrode while simultaneously grounding the drain electrodes. The mixing current I_{mix} was detected as a function of frequency and of the gate voltage V_g . The ground line was cut along the dashed line (*) to separate the drain from ground. An alternate drain is available in case a long nanotube grows across the junction. **(b)** Schematic cross-section of device, layers not to scale. The oxide thicknesses are 10 nm for the top gate and 1 μm for the back gate. The top gate has a slight overlap with the source contact. Catalyst pad not shown.

hysteresis in the gate voltage threshold (Kim, Javey et al. 2003). Setup and devices were kept at room temperature.

Mixing was obtained from a single ac source. The ac signal was applied to the source electrode of the device. It was combined with a dc bias by use of a high-frequency bias tee⁹, a component designed for superimposing dc and ac signals. This source dc bias was set to zero during the experiments in order to avoid dc sourcing of dc current¹⁰. The rectified signal was detected at the drain by means of a dc current amplifier¹¹. Finally, the gate was dc-biased independently from the source. The gate range was $-3 \text{ V} < V_g < 3 \text{ V}$ for most devices. This range was found not to induce dc current leakage to the gate.

Thanks to the bias tee, dc measurements were easily accomplished without taking the setup apart. By turning the ac source off, the dc conductance could be easily measured, allowing for analysis of the data by comparison with Equation 7.1.

7.4 Gate and power dependence of mixing

The dc conductances G_{dc} of two devices were measured at a dc bias of 10 mV and are plotted against gate voltage V_g in Figures 7.2 (a) and (b). The device of (a) is a p-type semiconductor since it turns on for negative V_g . The device of (b) is a small-bandgap semiconductor since there is a dip in the conductance as a function of V_g . The latter is also very conductive, at 60% of the quantum conductance limit of a nanotube¹².

⁹ Picosecond Model 5542.

¹⁰ Equation 7.1 predicts ac sourcing of dc/low-frequency current. Notice that both source and drain must be dc-biased (including zero) relative to each other in order for dc current to flow. A dc-floating terminal cannot source dc current.

¹¹ Ithaco 1201 low-noise current preamplifier.

¹² The quantum limit of a nanotube is $G_Q = 4e^2/h \sim 150 \mu\text{S}$, as discussed in Chapter 2.

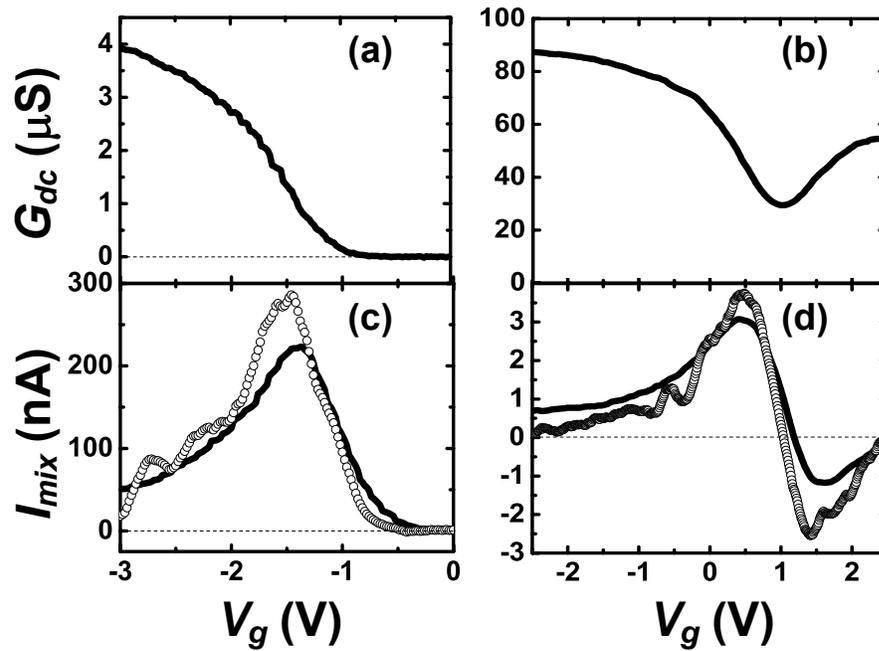


Figure 7.2. Correlation between experimental conductance and dc mixing current. **(a)** and **(b)** Conductance G_{dc} versus gate voltage V_g for a semiconducting and a small-bandgap device, respectively, for dc source-drain bias of 10 mV. Conductance of **(b)** is $\sim 60\%$ of the ballistic limit. **(c)** and **(d)** Mixing current I_{mix} versus V_g of devices **(a)** and **(b)**, respectively, at 10 MHz for $V_s^{ac,rms} = 400$ mV. In open circles are the numerical derivatives of **(a)** and **(b)**, respectively, scaled by the pre-factor of Equation 7.1. In **(d)**, a negative peak corresponding to the n-type FET behavior appears at $V_g \sim 1.5$ V. Reversal of the sign of the current is in agreement with Equation 7.1.

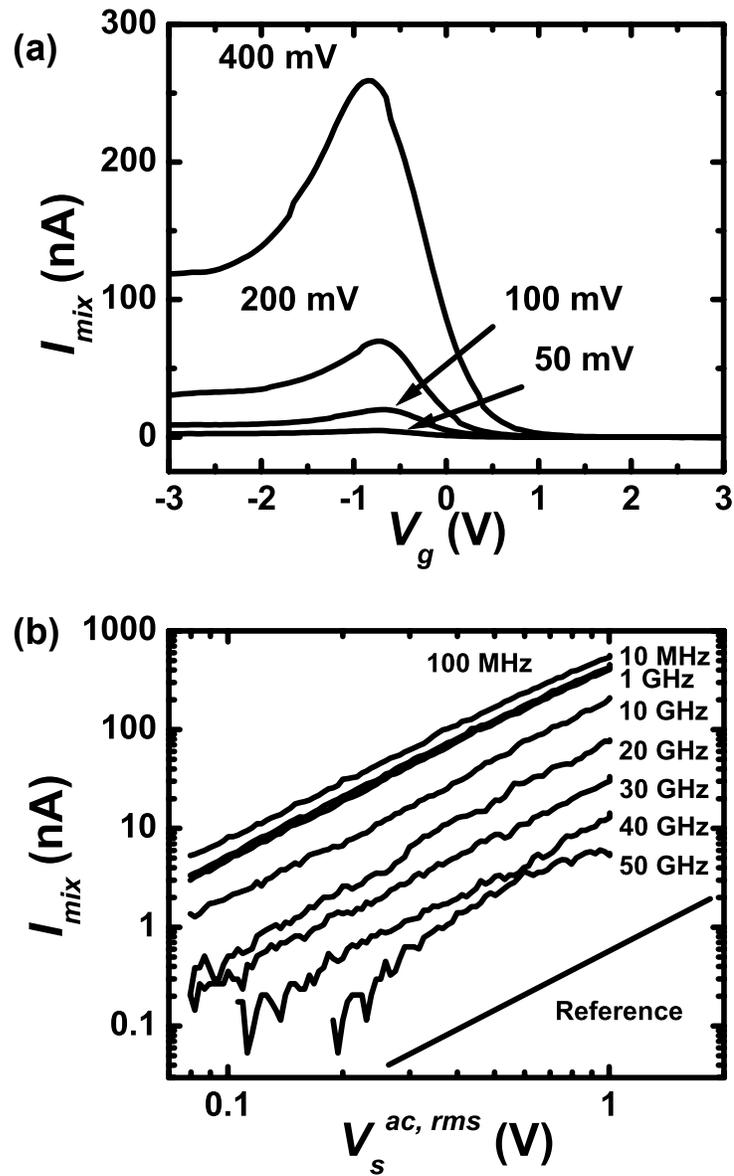


Figure 7.3. Amplitude dependence of mixing current. (a) I_{mix} versus gate voltage V_g for fixed frequency of 1 GHz and selected ac voltages (rms values). (b) Mixing current I_{mix} versus $V_s^{ac,rms}$, for a gate voltage near the peak. The ideal power-law line of 2 is shown for reference. Traces at 10 MHz and 1 GHz approximately overlap.

The dc mixing currents I_{mix} of the two devices are plotted (solid lines) against V_g in Figures 7.2 (c) and (d). The frequency used for mixing was 10 MHz and the ac power was -1 dBm, which corresponds to an ac amplitude of 400 mV rms¹³. The current I_{mix} resembles qualitatively the derivatives of the plots of Figures 7.2 (a) and (b), as predicted by Equation 7.1. Over 60 devices were measured, including both large- and small-bandgap semiconductors, and all displayed low-frequency mixing with similar relation to $\partial G_{dc}/\partial V_g$.

Figure 7.3 (a) shows I_{mix} versus V_g at different ac amplitudes (rms values), for the device of Figure 7.2 (a), at a frequency of 1 GHz. The amplitude of the peak follows a power law, as shown in Figure 7.3 (b). The mixing amplitude near the peak in $\partial G/\partial V_g$ is plotted against $V_s^{ac,rms}$ on a log-log scale at a variety of frequencies. The straight lines indicate that the response follows a power law in $V_s^{ac,rms}$ with an exponent in the range 1.9 to 2.2. The reference line indicates a quadratic law, as predicted by Equation 7.1.

The low-frequency experimental results are well described by the mixing expression, Equation 7.1. In this regime, we multiply the derivative of G_{dc} by the prefactor in Equation 7.1 to theoretically predict I_{mix} . The results are shown in open circles in Figures 7.2 (c) and (d). The amplitudes of the theoretical peaks are ~ 1.5 times greater than the experimental peaks at 10 MHz. This factor varied between 1 and

¹³ A power level of 0 dBm corresponds to 1 mW through the relation $P(\text{dBm}) = 10 \text{Log}_{10}(P(\text{mW}))$. This power level is defined assuming a 50 Ω impedance match to the internal impedance of the generator, such that $P = V_{rms}^2/50 \Omega$, where V_{rms} is the rms voltage seen at the output of the high-frequency source. When high impedance such as that of a nanotube is used instead, the ac voltage drop happens entirely across the device, and the voltage seen at the output becomes twice the nominal value. So -1 dBm corresponds to $V_{rms} = 200$ mV when 50 Ω -terminated, but $V_{rms} = 400$ mV in our case (high impedance).

1.5 for all the devices studied and is likely due to coupling losses¹⁴. We will discuss the origin of the sample-dependent discrepancies later in this chapter.

7.5 Frequency response of mixing current

Figure 7.3 (b) shows that the response varies with the square of the ac voltage. But Figure 7.3 (b) also shows that I_{mix} becomes smaller as the frequency increases. In order to investigate the mechanisms responsible for this amplitude decrease as a function of frequency, we mapped the mixing current versus frequency and gate voltage at an ac source power of -1 dBm for the device of Figure 7.2 (a), as shown in the color-coded plot of Figure 7.4 (a). The darkest red regions happen for $V_g \sim -1.2$ V and correspond to the peaks of individual gate traces such as that of Figure 7.2 (a). This shows that the gate location of the peak does not change with frequency¹⁵ and corresponds to the peak of $\partial G/\partial V_g$ at dc. The mixing amplitude at selected gate voltages versus frequency is shown in Figure 7.4 (c), obtained by performing vertical cuts in Figure 7.4 (a).

There is a periodic modulation of the mixing amplitude in Figure 7.4 (a) with frequency ~ 4.5 GHz. After looking into the properties of all the high frequency components in the ac line, this modulation was found to closely match the reflection properties of the GSG probe (as provided by the manufacturer) shown in Figure 7.4

¹⁴ Attenuation of high frequency components is measured by *Insertion Loss*, defined as $IL(\text{dB}) = -20 \text{Log}_{10}|T|$, where $|T|$ is the transmission amplitude through a component. The total transmission amplitude for this experiment is given by $|T|_{\text{BiasTee}}|T|_{\text{Cable}}|T|_{\text{Probe}}$. The joint transmission through the bias tee and cable (neglecting the probe) was measured with a network analyzer (scattering parameter S_{21}), resulting in $|T|_{\text{BiasTee}}|T|_{\text{Cable}} \sim 0.85$ at 1 GHz and ~ 0.22 at 40 GHz. Although this result corresponds to a 50 Ω termination, it illustrates that there are significant coupling losses coming from the setup. Maximum frequency ratings of individual high-frequency components typically correspond to the -3 dB threshold, at which point the output power is cut by half when 50- Ω terminated.

¹⁵ The gate threshold drifts over time due to hysteresis. Gate voltage traces at low and high frequency taken within a short window of time (to avoid drift) always showed the peak at the same location. To address this issue, the measurement of Figure 7.4 (a) was repeated several times, with drifts of the peak position of as much as 200 mV observed in between and during measurements. The one displayed in Figure 7.4 (a) had the least amount of drift. Notice that the position of the peak drifted relative to the measurements of Figure 7.2 (a) and Figure 7.3 (a) for the same device.

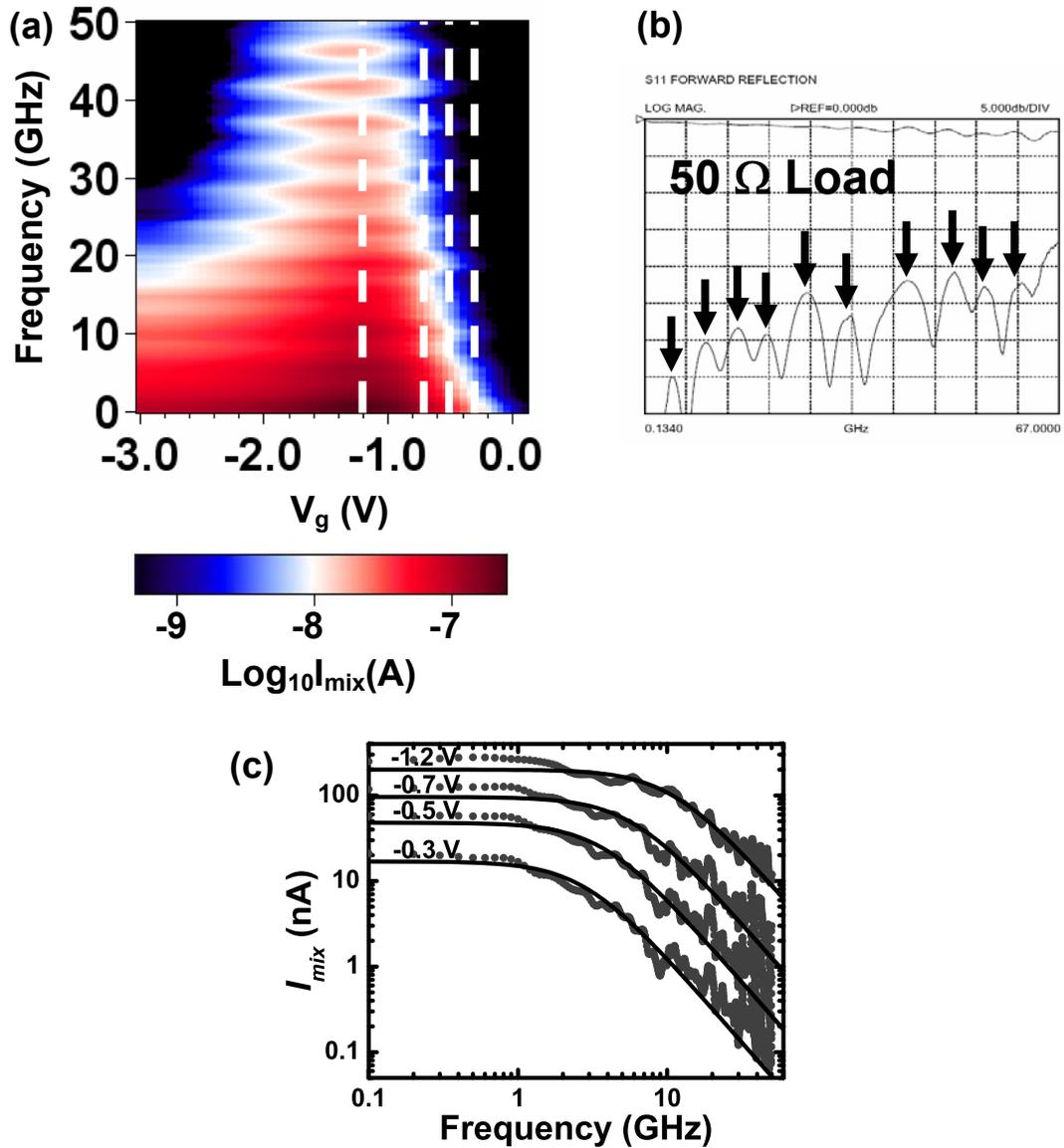


Figure 7.4. Damping of mixing current I_{mix} as a function of frequency. (a) Current versus gate voltage and frequency, for $V_s^{ac,rms} = 400$ mV plotted as a color scale. The beat with ~ 4.5 GHz period is likely due to standing waves in the external circuit, as shown by the red arrows in (b), corresponding to points of maximum reflection according to factory specifications of the GSG probes (GGB Industries). (c) I_{mix} versus f at selected gate voltages (white dashed lines in (a)). Black solid lines correspond to the numerical fit assuming a first-order low-pass filter. Cutoff frequency decreases from ~ 10 GHz at $V_g = -1.2$ V to ~ 3 GHz at $V_g = -0.3$ V.

(b). When terminated in 50Ω , the reflected power is low (~ -30 dB, of order 0.1%), and there is a modulation with small amplitude and with the same frequency as observed in the mixing experiment. Since the nanotube has such high impedance, the overall power reflected from the device should be close to 100%. The effect of the modulation over the ac voltage delivered to the source is then considerably amplified.

7.6 Model of frequency dependence of mixing

The simplest model used to describe the amplitude decrease as a function of frequency is that of a low-pass RC filter. By use of Equation 7.1, we can write the frequency dependence as:

$$\frac{I_{mix}(\omega)}{I_{mix}(\omega \rightarrow 0)} = \left| \frac{V_{out}}{V_{in}} \right|^2 = \frac{1}{1 + (\omega\tau)^2}, \quad (7.2)$$

where V_{out}/V_{in} represents the ac voltage gain and τ is a phenomenological RC constant¹⁶. We then use this expression to fit the data of Figure 7.4 (c), obtaining the solid curves. The cutoff frequency – which is set by the RC constant – is in the gigahertz range and depends on gate voltage. The damping tail falls off at ~ 20 dB/decade, just as expected for the voltage gain of a low-pass filter.

This RC constant was measured as a function of the gate voltage from the fits of I_{mix} versus frequency using Equation 7.2. The result is displayed in Figure 7.5, along with the dc conductance. The conductance was extracted from Figure 7.4 (a) by numerical integration of the low-frequency (10 MHz) mixing current according to

¹⁶ We have assumed that the ac conductance of the nanotube is similar to the dc conductance, such that the ratio of the derivatives is either close to unity or does not vary strongly with frequency compared to the square of the voltage ratio. Some evidence for this behavior has been observed recently in metallic nanotubes (Yu and Burke 2005).

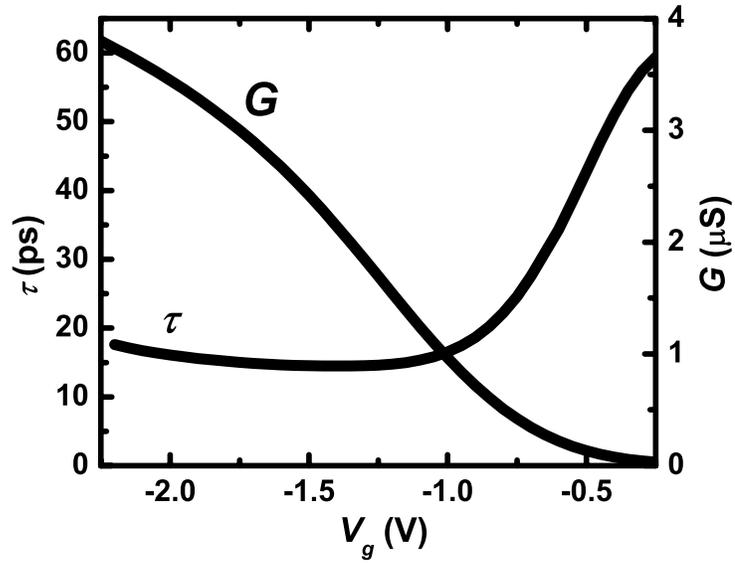


Figure 7.5. Time constant τ plotted against gate voltage. τ is roughly constant in the conductive state (see plot of conductance G_{dc}) due to the contacts. As the device turns off (positive gate voltage), τ increases. The plot for G_{dc} was taken with the same voltage threshold as the frequency plot in Figure 7.4 (a), which drifted slightly relative to the data in Figure 7.2 (a).

Equation 7.1¹⁷. We see from Figure 7.5 that $\tau \sim 15$ ps and is roughly constant while the device is highly conductive, but it increases when the resistance of the device becomes greater than ~ 1 M Ω . This indicates that the bulk resistance of the nanotube plays a major role in attenuation of I_{mix} near turn-off.

We determined the spread of values of τ for our devices by measuring the RC constant at the mixing peak for 16 devices (power of -1 dBm). The effect of the series resistance of the devices was also investigated. We applied a voltage to the substrate¹⁸ in order to gate the sections of the nanotubes not covered by the top gate. The resistances and time constants were measured when the back gate voltage was changed from $V_{bg} = -10$ V to $V_{bg} = +10$ V. The time constants at the mixing peak are plotted in Figure 7.6 against the estimated¹⁹ mixing peak resistances R_{peak} . The resistance of nine of these devices changed with an accompanying time constant change (shown by connecting arrows). Another five had no change of resistance. The time constants of the remaining two devices were not measured at $V_{bg} = +10$ V. Overall we found τ in the 7-28 ps range, while R_{peak} was found in the 8 k Ω - 700 k Ω range²⁰ – two orders of magnitude difference^{21,22}. There appears to be no direct correlation between the two variables. There also appears to be no correlation between the increase of the series resistance and the direction of change of the time constant.

¹⁷ The dc conductance as shown in Figure 7.2 (a) was used as the amplitude integration reference. The actual conductance never changed during measurements, therefore its maximum and minimum should be constants. Direct comparison with Figure 7.2 (a) is inaccurate due to the considerable drift of the gate conduction threshold between the measurements of Figures 7.2 and 7.4. Numerical integration provides a way of eliminating the drift from the analysis.

¹⁸ The intrinsic silicon substrate has thermally-activated carriers at room temperature. Despite its large resistivity, a dc bias can still be effective in gating parts of the device not covered by the top gate.

¹⁹ Measured at the steepest point of the corresponding G_{dc} .

²⁰ The sample included 6 pure semiconducting and 10 small-bandgap devices.

²¹ At low temperatures, the HRSi substrate is intrinsic, behaving as a really good insulator. The mixing peak time constant, however, remained in the same range when the device was probed at $T = 4$ K. This suggests that the pad-substrate capacitance (or absence of) does not affect the roll-off.

²² Measurements at low temperature were done in the dark to avoid optical excitation of carriers in the substrate. In the dark, the portion of the nanotube not covered by the local gate was found to be insensitive to a dc substrate voltage.

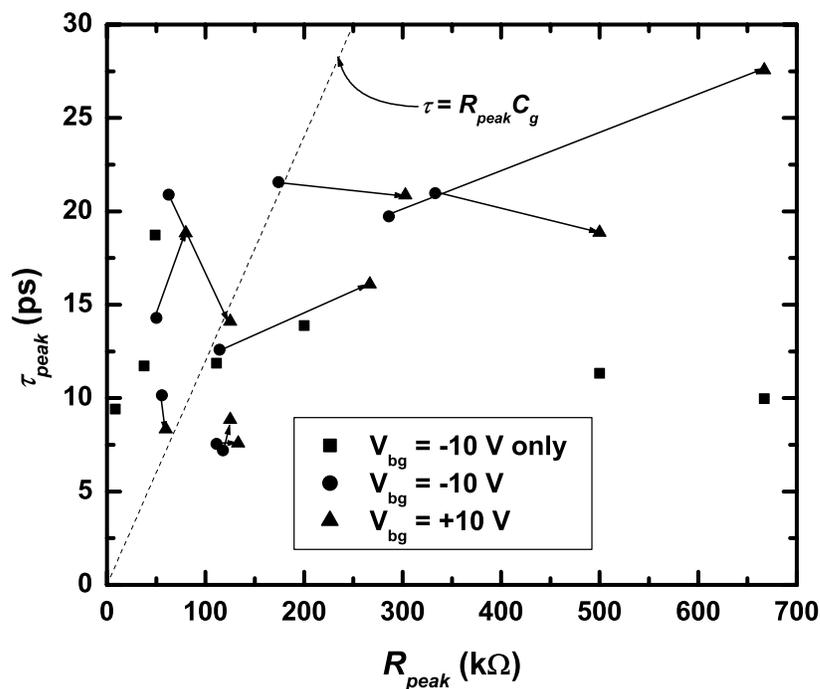


Figure 7.6. Time constant τ at the mixing peak versus resistance R_{peak} at the mixing peak. The time constant was measured for a total of 16 devices, of which 6 were pure semiconductors and the remaining 10 were small-bandgap semiconductors. The substrate voltage V_{bg} was kept at -10 V. The effect of a change of V_{bg} to +10 V is shown for nine of these devices (hence a total of 23 points) and illustrated by the connecting arrows. There appears to be no direct correlation between the peak resistance and the time constant.

For the device of Figure 7.5, the observed time-constant in the on-state of 15 ps with $C_g \sim 1.2 \times 10^{-16}$ F as the gate capacitance²³ gives a resistance $R \sim 125$ k Ω . This time constant is often less than the RC time of the device, as seen by the dashed line in Figure 7.6. We will now make use of the model introduced at the end of Chapter 4 that describes the roll-off of the mixing current of a one-dimensional distributed mixer in the RC operation limit. To summarize, we predicted that the cutoff frequency is a function of the resistances of the contacts and the bulk. According to the model, the ultimate limit of the cutoff frequency happens in the on-state (comparable bulk and contact resistances) and is given not by the total resistance, but by the resistance of the source contact R_s . Since $R_s \leq R_{total}$, then $\tau \leq R_{total}C_g$. This condition specifies the upper bound of the time constant and conversely the lower bound of the cutoff frequency. The cutoff frequency may also change as a function of overvoltage, but the precise trend depends on the relative magnitudes of each of the resistances.

The source resistance limit in the on-state agrees with the results of Figure 7.5. The measured time constant of 15 ps in the conductive state corresponds to a resistance that is lower than the on-state resistance R_{on} . Since the contact resistances account for a fraction of R_{on} , the time constant may be contact-limited. Near turn-on, on the other hand, the total resistance is considerably larger than 1 M Ω and we observe that the time constant increases. The model shown in Figure 4.10 predicted that when the resistance of the bulk dominates the total resistance, the frequency cutoff should *increase* – time constant should *decrease*. One possibility for this disagreement is that we do not find ourselves in the same regime described by the simulation, but in some intermediate state where the time constant is allowed to increase relative to its value in the on-state. That could be either due to Schottky

²³ The capacitance was measured independently with a capacitance bridge (Ilani and Donev 2005), giving $C_g \sim 6 \times 10^{-17}$ F/ μm . The gated length of device was ~ 2 μm .

contacts (resistance of the contacts already significant near turn-on and modulated by the gate voltage) or due to a non-uniform conductance. This last possibility could be a consequence of disorder near turn-on or partial coverage of the top gate (which gates efficiently the middle section of the nanotube but not its ends).

The theoretical constraint $R_{total}C_g$ at the mixing peak ($R_{total} = R_{peak}$) is represented by the dashed line in Figure 7.6. We observe that the experimental results do not agree with this analysis for the six devices with time constants lying above the line. This corresponds to lower cutoff frequencies for these. A simple explanation for this observation is that there is an external, setup-related cutoff. Also notice the devices with time constant above the line are the most conductive ones, with peak resistances below 100 k Ω .

Comparison with the model of distributed mixing of Chapter 4 appears to be of limited use in analyzing the available experimental data. In spite of this, the experimental results do not entirely disprove the model. More must be done to understand the origins of the observed cutoffs of mixing.

7.7 Schottky mixing

At high overvoltages, the resistance of the device approaches a constant value. This is typically due to comparable bulk and contact resistances (Zhou, Park et al. 2005). Then the voltage drop of the bulk of the nanotube can be significantly reduced from the total, according to:

$$\Delta V_{bulk} = \frac{R_{bulk}}{R_{tot}} \Delta V_{tot}, \quad (7.3)$$

where R_{bulk} and R_{tot} are the resistances of the bulk and of the entire device, respectively. Then, the mixing current originated in the bulk becomes negligible due to the decrease of the voltage drop and of $\partial G(\omega)/\partial V_g$ (see Equation 7.1). In this limit, the nonlinearities from the contacts become more pronounced (Heinze, Tersoff et al. 2002). In order to study this regime, we concentrate on the on-state region of p-type operation, such as $V_g \sim -3$ V in Figure 7.2 (a).

Figure 7.7 (a) shows mixing at 50 GHz for the device of Figure 7.2 (a). Although the amplitude of the current at 50 GHz is ~ 20 times smaller than that at 10 MHz, the gate dependence still follows $\partial G_{dc}/\partial V_g$ for $V_g > -2$ V. The current levels detected are still well within our experimental sensitivity and there is no sign of deviation of $\partial G(\omega)/\partial V_g$ from its dc value for $V_g > -2$ V. The mixing current of this device at $V_g = -3$ V is also plotted versus frequency in part (b). We see that the mixing current becomes negative at high frequencies. It also appears to be relatively constant.

We plot I_{mix} versus V_g in Figure 7.8 for a small-bandgap nanotube device, as illustrated by the G_{dc} versus V_g curve. The frequency was again 10 MHz and the ac source power was -1 dBm. We measured I_{mix} by probing each end of the device with the ac probe. When the ac probe was placed at the end labeled (1), the mixing current at $V_g = -3$ V was positive. It changed to negative when end (2) was probed instead. The remaining gate dependence, however, remained the same.

The gate dependence at 50 GHz of I_{mix} in Figure 7.7 (a) can be explained by Schottky mixing. A crossover to negative mixing current in p-type operation is predicted neither by means of our theory of distributed mixing or by Equation 7.1 for a discrete mixer. This result is however consistent with the Schottky theory: we predicted that for contacts with similar nonlinear behavior (characterized by the voltage range in which they behave nonlinearly), the mixing current is dominated by the contact with the largest resistance at low frequencies, but it becomes entirely

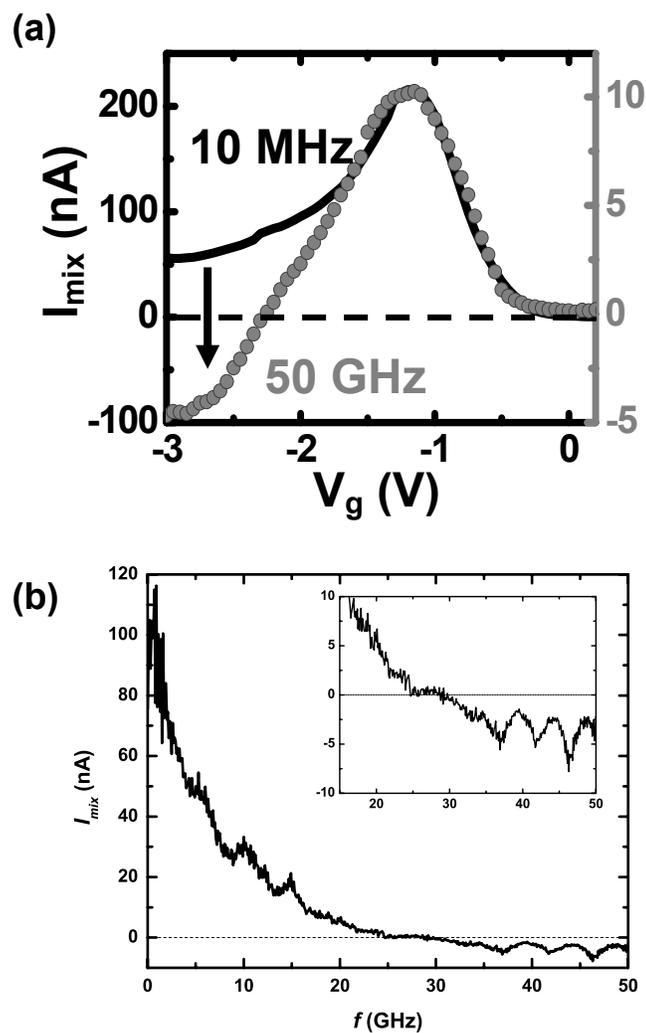


Figure 7.7. Contact effects at negative gate voltage. **(a)** Mixing signal at 10 MHz and 50 GHz, currents in nA (black = 10 MHz = left; gray = 50 GHz = right). Current becomes negative at high frequencies in the region of constant dc conductance. **(b)** I_{mix} versus frequency for the device of part (a), measured at $V_g = -3$ V. At this gate voltage, $\partial G/\partial V_g$ goes to zero and I_{mix} is dominated by the Schottky contacts. For $f > 30$ GHz (inset), I_{mix} becomes negative. It also appears relatively constant. Further work is necessary to determine if the device is mixing with constant amplitude or if the attenuation from the setup is playing a role.

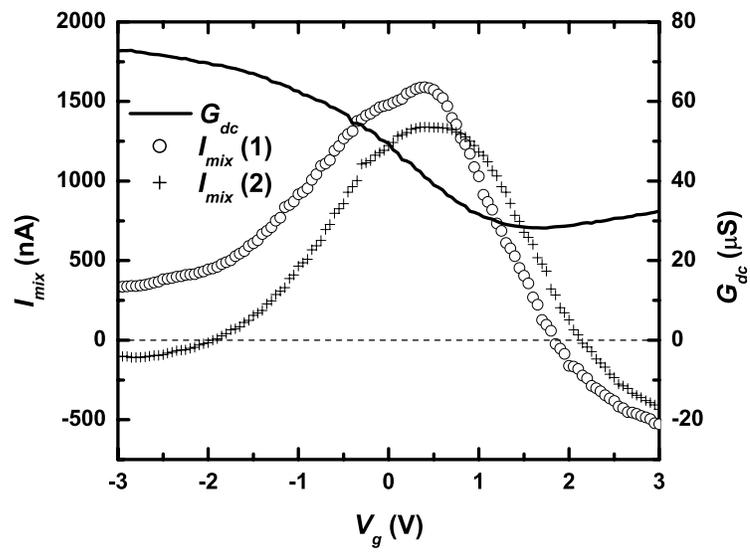


Figure 7.8. Conductance and dc mixing current of a small-bandgap nanotube versus gate voltage. I_{mix} was measured by applying the ac voltage to the opposite ends of the device (labels 1 and 2). The sign of I_{mix} is different at $V_g = -3$ V due to the asymmetry of the contacts.

dominated by the source contact at high frequencies (and negative, due to its reverse-biased nature). The theory also predicts that it does not change frequency²⁴. Although Figure 7.7 (b) shows a constant mixing current at high frequencies, further work is needed in order to determine if this is because mixing is constant or if it appears to be constant due to cancellation between the Schottky mixing and the attenuation of the signal by the setup.

Finally, we analyze the reversal of the current sign in Figure 7.8 when the ac voltage was applied to either source or drain. The asymmetry of the current is again consistent with the Schottky theory. Since the Schottky contacts behave as reverse-biased diodes, negative mixing current would be favored by default. Yet, we predicted that at low frequency, mixing would be dominated by the most resistive contact. This means that end (2) was the more resistive of the two, since it overcame the natural tendency of contact (1) to generate negative current and dominate mixing. This was typically the case with most of the devices studied.

7.8 Conclusions

In this chapter, we investigated the high-frequency performance of carbon nanotube transistors with a mixing technique using a dc detection scheme. This technique works with semiconducting and small-bandgap devices. When the nanotube transistor operates as a mixer, the mixing current depends on the derivative of the conductance with respect to the gate voltage and on the magnitude of its associated voltage drop according to Equation 7.1. At larger overvoltages, mixing is dominated by the Schottky contacts. In this regime, Schottky mixing makes the current negative at high frequencies.

²⁴ In the absence of strong capacitive parasitics, the diode is just a resistor. At high frequencies, the gate shorts the ac signal to ground through the gate and all the mixing comes from the source contact only.

The frequency dependence of the mixing current showed a cutoff frequency in the range 1-10 GHz. This is in order-of-magnitude agreement with the distributed mixer model presented in Chapter 4. The model predicted a minimum cutoff frequency limited by the RC time associated with the resistance of the source contact and the gate capacitance of the nanotube. Nevertheless, if the time constant of the setup is comparable to that of the device, the setup sets the cutoff frequency instead. Further work is needed in order to clarify this issue.

The ac experiments that we have reported here were done at the highest frequencies so far for single²⁵ nanotube transistors. We have measured their response up to 50 GHz, and we have found them still to be mixing at this frequency. This could be useful for an application such as a nanoscale ac power detector.

²⁵ Our samples have a small number of nanotubes per junction. Although we design our junctions for one nanotube bridging the gap between the electrodes, we often find two or three (but rarely more than five).

CHAPTER 8

CONCLUSION

8.1 Summary

We have explored the ultimate room-temperature limits of electrical performance of single-walled carbon nanotube field-effect transistors (FETs) in the dc gating regime and in the RC limit of mixer operation. These experiments demonstrated some of the limiting factors that are relevant for technological applications of nanotube transistors.

In Chapter 6 we demonstrated the dc gating limits of single-walled carbon nanotube transistors by means of an electrolyte gate. Using the dielectric and insulating properties of the solution in combination with the short screening lengths of the ions, we have shown that the electrolyte gate capacitor reaches the quantum limit of operation as introduced in Chapter 2. This is the best gating performance that can be obtained by use of a carbon nanotube transistor. This property is particularly important for sensing applications: the conductance of a carbon nanotube FET should be affected by local charges in a manner analogous to a gate electrode.

The ac electrical properties of carbon nanotube transistors were studied by using them as mixers/rectifiers at frequencies up to 50 GHz, as reported in Chapter 7. This is the highest operational frequency reported so far for nanotube transistors. We have found that the experimental mixing response of samples with minimized parasitic capacitances had a cutoff at frequencies in the 1-10 GHz range. We interpreted these experimental results with the circuit theory developed in Chapter 4. Our analysis with a model using the distributed nature of the capacitance and resistance of the nanotube suggests that the frequency cutoff is determined by the contacts. The experimental

results do not rule out this possibility but do not confirm it entirely either. A possibility for the discrepancy is that the setup contributes to the cutoff. Further work is necessary to resolve this issue.

8.2 Future directions

Carbon nanotubes are currently exciting materials for building high-performance electronics. By showing the gating limits of the transistors, we have paved the way to optimization of the gate geometries and charge sensing applications. In the high-frequency limit, we have shown that maximum operating frequencies might be raised if the properties of the contacts are optimized.

We will finish this thesis discussing two potential experiments based on the high-frequency work that was presented here. The first one follows from the theory of distributed mixing. The analysis of Chapter 4 showed that a dc voltage profile must build up along the nanotube in order to sustain the mixing current. We simulated the profile of this dc voltage along the device when the resistance of the bulk dominates the total resistance (see Figure 4.8). We found that the profile was symmetric at frequencies below $\sim (2\pi RC)^{-1}$, where R is the resistance of the bulk and C is the gate capacitance. We also found that the voltage peaked in the center of the nanotube at these frequencies, with an amplitude of approximately $\frac{1}{4}RI_{mix}$, where I_{mix} is the total dc mixing current. Above the cutoff determined by the bulk, we found that the voltage profile should become asymmetric and peak near the source contact with an increasing amplitude (the maximum amplitude being RI_{mix} at very high frequencies).

In order to estimate the experimental value of the built-up dc voltage peak we will assume the mixing current to be that of the mixing peak, which for semiconducting nanotubes can happen near turn-on (bulk dominates total resistance and voltage profile). We found experimentally that a typical mixing peak current of \sim

1 μA can be obtained at an ac source voltage of ~ 0.5 V (peak voltage). For the semiconducting device of Chapter 7, that corresponded to a bulk resistance of ~ 1 M Ω , still reasonably larger than the resistance of the contacts. Using a gate capacitance of $\sim 10^{-16}$ F for a 2 μm -long nanotube, the voltage profile frequency cutoff would be $(2\pi RC)^{-1} \sim 1.5$ GHz. It should be possible to make devices with lower cutoff by growing longer nanotubes – a 10 μm -long nanotube would have a cutoff around 50 MHz. We then find that at frequencies below the cutoff the maximum voltage should be $\sim \frac{1}{4}RI_{mix} \sim 0.25$ V dc. We postulate that it should be possible to verify this by means of a scanning probe technique such as electric force microscopy (EFM), as described by Bachtold et al. (Bachtold, Fuhrer et al. 2000; also consult Girard 2001 for an accessible summary of the technique). Detection of the built-up dc voltage profile would constitute a direct measurement of the frequency dependence of distributed mixing of a nanotube.

The second and last experiment that we propose here is concerned with the transmission-line limit of operation. In this regime, transport should be ballistic in the bulk of the nanotube. Due to the negligible resistance of the bulk, the nanotube should behave as an LC line. If there were Schottky contacts at the ends, a mixing current would result. We postulate that Schottky mixing could serve as a probe to detect the plasma waves – collective excitations that originate from the LC resonances. This experiment would be very important as a direct observation of the physics of nanotubes in the lossless limit. It has been suggested (Burke 2002) that a short nanotube (few microns long) would exhibit such resonances in the terahertz regime (optical range). On the other hand, long nanotubes (100 μm) would have resonances in the gigahertz regime that could be detected electronically with equipment such as that used in the experiment of Chapter 7. Although long nanotubes can now be routinely grown, it is unlikely that they would be able to retain ballistic transport throughout

their entire lengths, in particular because they would also need to be free of localized defects. Experiments are currently under way to perform plasmon detection using an antenna design with Schottky mixing as the detection scheme (Zhong 2005).

APPENDIX

A.1 Mixing expression

We will now derive the distributed mixing current of a nanotube when both contact resistances are taken into consideration. We start with the definition of the propagation constant from Chapter 4, $\gamma = [j\omega\rho C']^{1/2} = (1+j)\gamma_0$, where j is the imaginary constant and ρ and C' are the nanotube's resistivity and capacitance per unit length, respectively. The real and imaginary parts are equal to $\gamma_0 = [\omega\rho C'/2]^{1/2}$, and we define additionally the product $x = \omega RC$, so that we can write $\gamma_0 L = [x/2]^{1/2}$, where L is the length of the nanotube. In order to simplify the algebra, we define the ratio between the contact resistance of the drain and the nanotube's bulk resistance as $\chi_d = R_d/R$, in order to define the ratio $\eta_d = \chi_d[2x]^{1/2}$. The characteristic impedance of the line is $Z_0 = \rho/\gamma$, with which we write the reflection coefficient at the drain end:

$$\Gamma(L) = \frac{R_d - Z_0}{R_d + Z_0} = \frac{\eta_d^2 - 2 + 2j\eta_d}{\eta_d^2 + 2\eta_d + 2}. \quad (.1)$$

Next, we integrate Equation 4.30 using the dc division rule of 4.10:

$$I_{mix} = -\frac{1}{2} \frac{\partial G}{\partial V_g} \frac{1}{1 + \chi_s + \chi_d} \int_0^L \text{Re} \left[V^*(z) \left(-\frac{\partial V(z)}{\partial z} \right) \right] dz, \quad (\text{A.2})$$

where $\chi_s = R_s/R$ is the ratio between the contact resistance of the source and the nanotube's bulk resistance, the voltage profile from source to drain is $V(z)$, G is the conductance of the bulk and V_g is the gate voltage. We then relate the reflection coefficient at the source ($z = 0$) to the one at the drain with $\Gamma(0) = \Gamma(L)e^{-2\gamma L}$ to write:

$$I_{mix} = -\frac{1}{2} \frac{\partial G}{\partial V_g} \frac{e^{-2\gamma_0 L}}{1 + \chi_s + \chi_d} \left| \frac{V(0)}{1 + \Gamma(0)} \right|^2 \cdot \left[\left(e^{\gamma_0 L} - |\Gamma(L)|^2 \right) \sinh(\gamma_0 L) - 2(\sin(\gamma_0 L) \operatorname{Re} \Gamma(L) - \cos(\gamma_0 L) \operatorname{Im} \Gamma(L)) \sin(\gamma_0 L) \right], \quad (\text{A.3})$$

where we used Equation 4.28 for $V(z)$. By use of Equation 4.27, we can relate the amplitude $V(0)$ to the input ac signal V_{sd} and write:

$$\left| \frac{V(0)}{1 + \Gamma(0)} \right|^2 = \frac{2V_{sd}^2}{\left[1 + \operatorname{Re} \Gamma(0) + \operatorname{Im} \Gamma(0) + \eta_s (1 - \operatorname{Re} \Gamma(0)) \right]^2 + \left[1 + \operatorname{Re} \Gamma(0) - \operatorname{Im} \Gamma(0) + \eta_s \operatorname{Im} \Gamma(0) \right]^2}, \quad (\text{A.4})$$

where we defined $\eta_s = \chi_s [2x]^{1/2}$.

Finally, we can calculate the cutoff of the mixing current once both ratios of the contact resistances to the bulk resistance are known. The frequency directly controls the parameter x . There is still an additional dependence of the result on $\partial G / \partial V_g$ and the amplitude V_{sd} of the input, which will correct the overall amplitude of mixing, but it does not influence the cutoff.

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