17.7 A 330μm×90μm Opto-Electronically Integrated Wireless System-on-Chip for Recording of Neural Activities

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Recording neural activity in live animals *in vivo* poses several challenges. Electrical techniques typically require electrodes to be tethered to the outside world directly via a wire, or indirectly via an RF Coil [1], which is much larger than the electrodes themselves. Tethered implants result in residual motion between neurons and electrodes as the brain moves, and limits our ability to measure from peripheral nerves in moving animals, especially in smaller organisms such as zebra fish or fruit flies. On the other hand, optical techniques, which are becoming increasingly powerful, are nonetheless often limited to subsets of neurons in any given organism, impeded by scattering of the excitation light and emitted fluorescence, and limited to low temporal resolution [2]. Here we present the electronics for an untethered electrode unit, powered by, and communicating through a microscale optical interface, combining many benefits of optical techniques with high temporal-resolution recording of electrical signals.

Figure 17.7.1 illustrates the concept of such a microscale, optically-transduced electrode site with I-V curves of a custom, dual-functioning AlGaAs Photo-Voltaic/Light Emitting Diode (PVLED) unit in its PV and LED modes, which is mounted on top of a CMOS die. About 98% of the time, the PVLED acts as a power source, transducing incoming light into electrical power, providing at least 1μA at ~0.9V. During the remaining ~2% of the time, the PVLED acts as an optical transmitter, emitting optical pulses to transmit encoded measurement data to an external receiver at a longer wavelength. This allows the system to be more compact than the previously reported RF [1] and ultrasonic [3,4] approaches. The bottom-right of the Fig. 17.7.1 depicts the integration of the PVLED on 180nm CMOS where the underlying CMOS circuitry incorporates recording electrodes, amplification, pulse-position encoding, and a PVLED interface to arbitrate power and communications [5]. Since neural tissue is primarily scattering (as opposed to absorbing), optical power and information can propagate well beyond the range of traditional optical imaging, allowing such a system to function at depths greatly exceeding that of imaging, but without the tethers required by most electrodes.

Figure 17.7.2 shows a block diagram of the proposed system and a schematic of the amplifier that boosts the differential signal between the two sensing electrodes that are spaced ~150μm apart to sample the electric fields generated by nearby neurons. Approximately one half of the total current from the PVLED (500nA of 1μA) is used to provide the low noise amplification through the input differential pair (M1 & M2). A pair of NFETs (M3 & M4) act as high-pass active loads: the amplifier output is fed back to the gates from through transistors acting as pseudo resistors and shunted by MOS capacitors. Thus, M3 and M4 provide a low impedance at low frequencies (<<1Hz) but a high resistance in the neural band of interest (>10Hz). Finally, a pair of diode-connected PFETs (M5 & M6) provide a matched load for a controlled mid-band gain, with parallel MOS capacitors setting a low-pass corner at about 10KHz to suppress higher-order aliasing terms. It should be noted that, because the high-pass load would lead to a prohibitively long start-up time while illumination may be transitory, the high-pass resistors are briefly set to a low resistance state during VDD startup, to rapidly calibrate out DC offsets and bias state before switching to their normal high-resistance state. The amplifier and all other circuits are biased from a supply-invariant PTAT-like current source to provide immunity to variations in VDD during fluctuations in illumination or output optical pulse generation.

We have implemented Pulse Position Modulation (PPM) for signal encoding for its high information-per-photon efficiency [6]. Figure 17.7.3 shows that the amplifier drives the pulse-position encoder where a 10KHz relaxation oscillator generates a periodic pulse, which charges capacitor C1 to VDD. After this reset, the capacitor is discharged by one of a pair of differential currents generated from the output of the amplifier. The result is a square-wave whose duty cycle reflects the inverse of the measured voltage. Fixed currents bound the duty cycle to a range between 20% and 80%. A T-flip-flop selects which of the two complementary currents discharges the capacitor at any given time, alternating between clock cycles – like chopping, this allows the separation of signals from fluctuations due to slow-changing light level. The resulting square-wave is passed through a delay-line of current-starved inverters, and edges are combined to generate pulses on both the rising and falling edges of the square wave. The timing of these signals is illustrated in Fig. 17.7.3. A wider pulse disconnects VDD from the PVLED for 1ms, and two other pulses switch a 3-capacitor (1.2pF each) charge pump, switching from a parallel configuration to a series configuration, and connecting to the PVLED to deliver a sharp (<100ns) current pulse. Each cycle of the relaxation oscillator generates two light pulses through the PVLED, one at the beginning of the cycle, and the other between 20μs and 80μs later, where this time difference denotes the input voltage. One extra benefit of using such low duty-cycle optical pulses (<0.1%) is that multiple units could be active simultaneously with minimal overlap between their pulse trains, where PVLEDs with different wavelengths can provide further disambiguation via wavelength multiplexing.

To ensure that the VDD does not drop excessively during the pulsing events (when it is disconnected from the PVLED), 16pF of decoupling capacitance is installed. In addition, because the PVLED can only supply a finite amount of instantaneous current, and to avoid an excessive supply ripple, the charge pump capacitors are recharged slowly over ~10μs. A 20μs minimum pulse spacing ensures that the charge pump is fully charged before each pulse. Finally, to ease the assembly of PVLED and CMOS, a cross-coupled rectifier (polarity corrector) is implemented to ensure the system functionality regardless of the polarity of the PVLED on its pads.

The CMOS circuit is fabricated in 0.18μm CMOS, with an active area of 210μm × 90μm. For testing, we have bonded the CMOS to a PVLED. When we illuminate the hybrid system with ~50nW/μm^2 of band-passed white light (380nm–720nm), which is about 1/6th of the safe limit for brain tissue [7], light pulses are measured as expected as shown in the top-left of Fig. 17.7.4. Figure 17.7.4 also shows that the pulse-position modulated optical pulses can be demodulated to reconstruct a 1KHz test input signal applied to the input electrodes. The system has a transduction gain of ~70ns/μV across 1Hz to 10KHz and the gain compresses for inputs larger than 6mV_{PP} (2.1mV_{RMS}), whereas the input-referred noise floor is ~42μV_{RMS}. We examine the wake-up characteristics of the system for its potential use in pulse-powered environment (as opposed to continuous exposure). Figure 17.7.5 (left) demonstrates that our system wakes up in under 1ms.

Finally, to demonstrate the system's capability to encode real neural signals, we have connected the input electrodes to the ventral nerve cord of an earthworm using probes, with a commercial neural amplifier connected in parallel to provide a reference baseline. Figure 17.7.5 (right) clearly shows that the composite spikes have been accurately encoded in the output optical pulses, even when communication and power are purely optical.

Figure 17.7.6 shows a breakdown of the design by power consumption (top-left) and by silicon area (top-right). As emphasized earlier, the power consumption is dominated by the main amplifier and the charge pump. Area is dominated by the amplifier (for lower flicker noise), LED driver, and decoupling. The bottom of the Fig. 17.7.6 shows a table of comparison against prior art.

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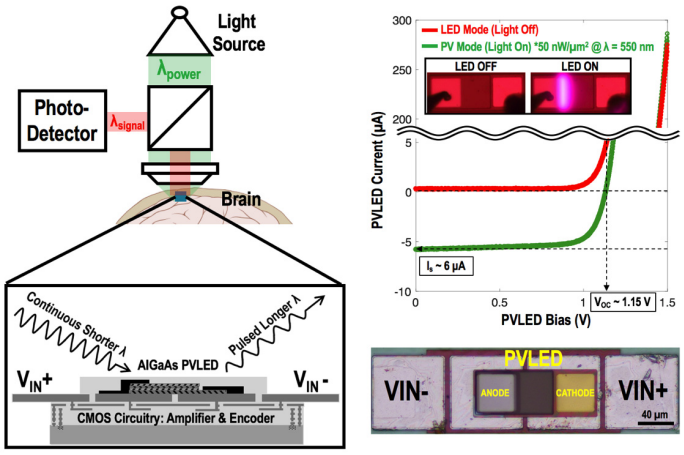


Figure 17.7.1: Left: an envisioned implementation of the system. Top-right: characterization of a micro-scale AlGaAs diode device utilized as PV as well as LED. Bottom-right: a micrograph of an assembled system.

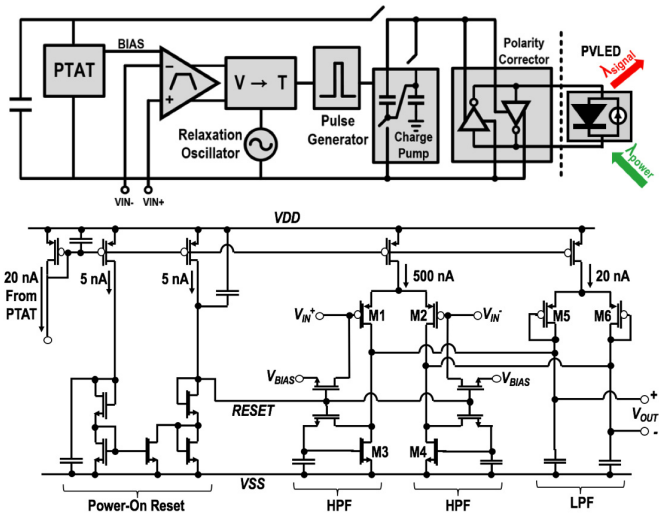


Figure 17.7.2: Top: block diagram of the proposed system. Bottom: schematic of the amplifier used, including the startup circuit and filtering.

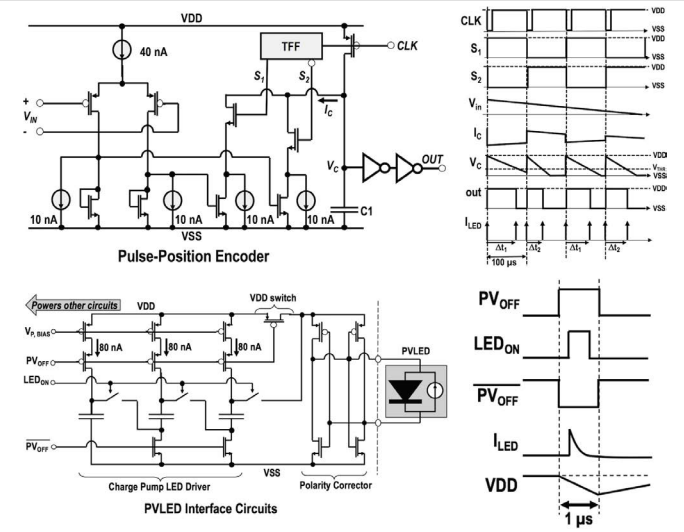


Figure 17.7.3: Top: the PPM encoder and associated timing diagram. Bottom: the pulse generator and its associated timing diagram.

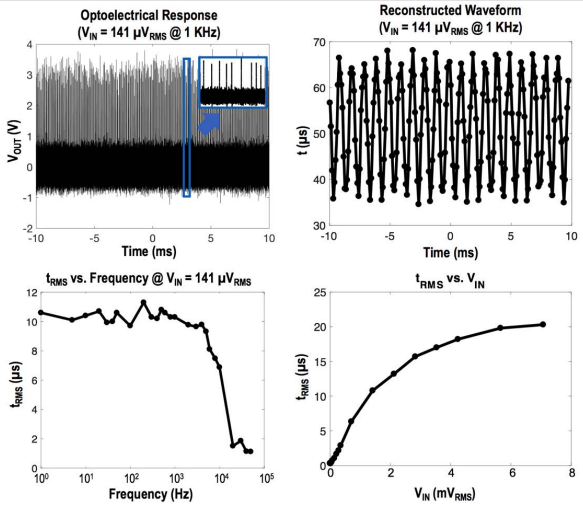


Figure 17.7.4: Example measurement of optical output pulse (top-left), and associated reconstructed 1KHz waveform (top right). Bottom: signal gain as a function of frequency (left) and amplitude (right).

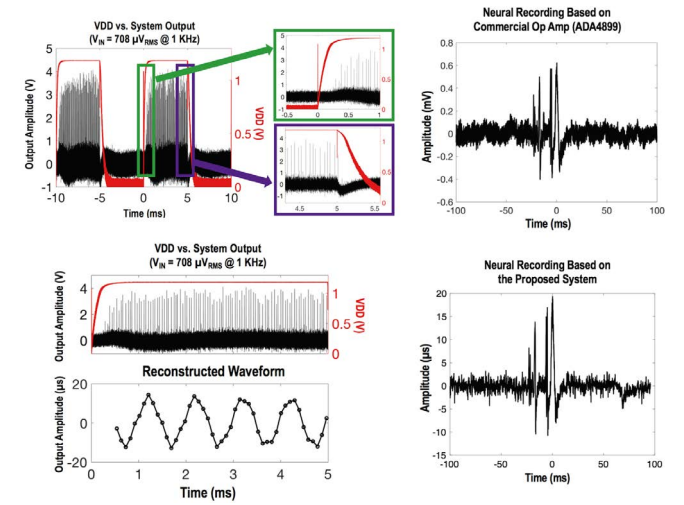
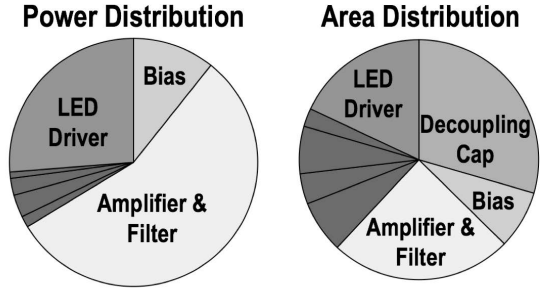


Figure 17.7.5: Left: start-up, showing optical pulses (top) and decoded signal (bottom). Right: neural recording on an earthworm ventral nerve using a commercial amplifier (top) and the presented system (bottom).



	Integrated Neural Interface [1]	Neural Dust [4]	This Work
Wireless Power Source	RF Coil	Ultrasonic	Optical
Gain (dB)	60	N/A	24
Bandwidth (KHz)	5	> 30	10
Noise Floor (μV_{RMS})	5.1	180	42
No. of Channels	100	1	1
Power per Channel	135 μW	0	< 1 μW
Volume per Channel (mm^3)	> 10	2.4	< 0.01

Figure 17.7.6: Top shows the power and area breakdown of the presented work. Bottom tabulates the comparison against prior art.

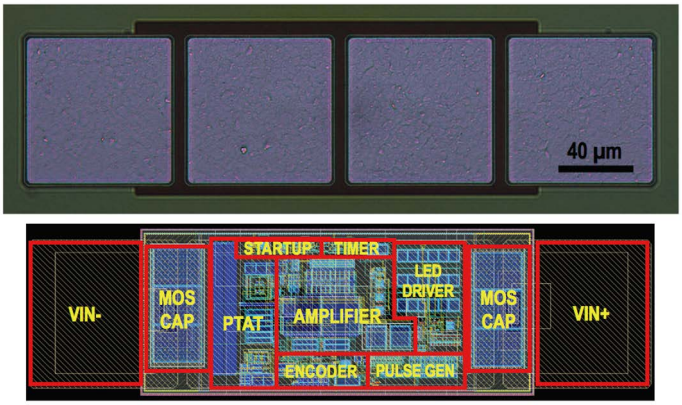


Figure 17.7.7: Top: die micrograph of the 180nm CMOS die, bottom: corresponding layout with circuitry annotated.

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